MT7976DAN Datasheet

802.11ax Wi-Fi RF Chip

Version: 1.4

Release date: 2021/11/15

Document Revision History

Revision	Date	Author	Description
V1.0	2021/10/22	TM Chen	1. Initial version.
V1.1	2021/10/25	TM Chen	Correct typo for Pin8, 114,120,126
V1.2	2021/11/05	TM Chen	Update the Pin name for PA VDD=1.8V
V1.3	2021/11/08	TM Chen	1. Update TOP marking to MT7976AN for QFN 2. Update supporting frequency band to 5/6GHz
V1.4	2021/11/15	TM Chen	POD modified

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Lists of Figures and Tables

1 System Overview

1.1 Functional Block Diagram

MT7976DAN is an IEEE WiFi 6 MIMO RF chip which contains 2.4 GHz WI-Fi transceiver front-ends and 5 GHz Wi-Fi transceiver front-ends in a DRQFN package. Simplified block diagram and how MT7976DAN is used are shown in Figure 1-1. The top control logics control each subsystem independently. Each subsystem also has dedicated LDOs. A thermal sensor and a low-speed ADC (Analog-to-Digital Converter) are provided to monitor MT7976DAN's temperature variation. MT7976DAN has its dedicated crystal oscillator (XO) circuit. Besides, XO circuit provides an external clock source to other chips in the platform.

The transceiver front-ends are on MT7976DAN while the ADC/DAC (Analog-to-Digital Converter/Digital-to-Analog Converter) is in the companion modem chip. The interface drivers/receiver buffers are designed to drive PCB trace loading.

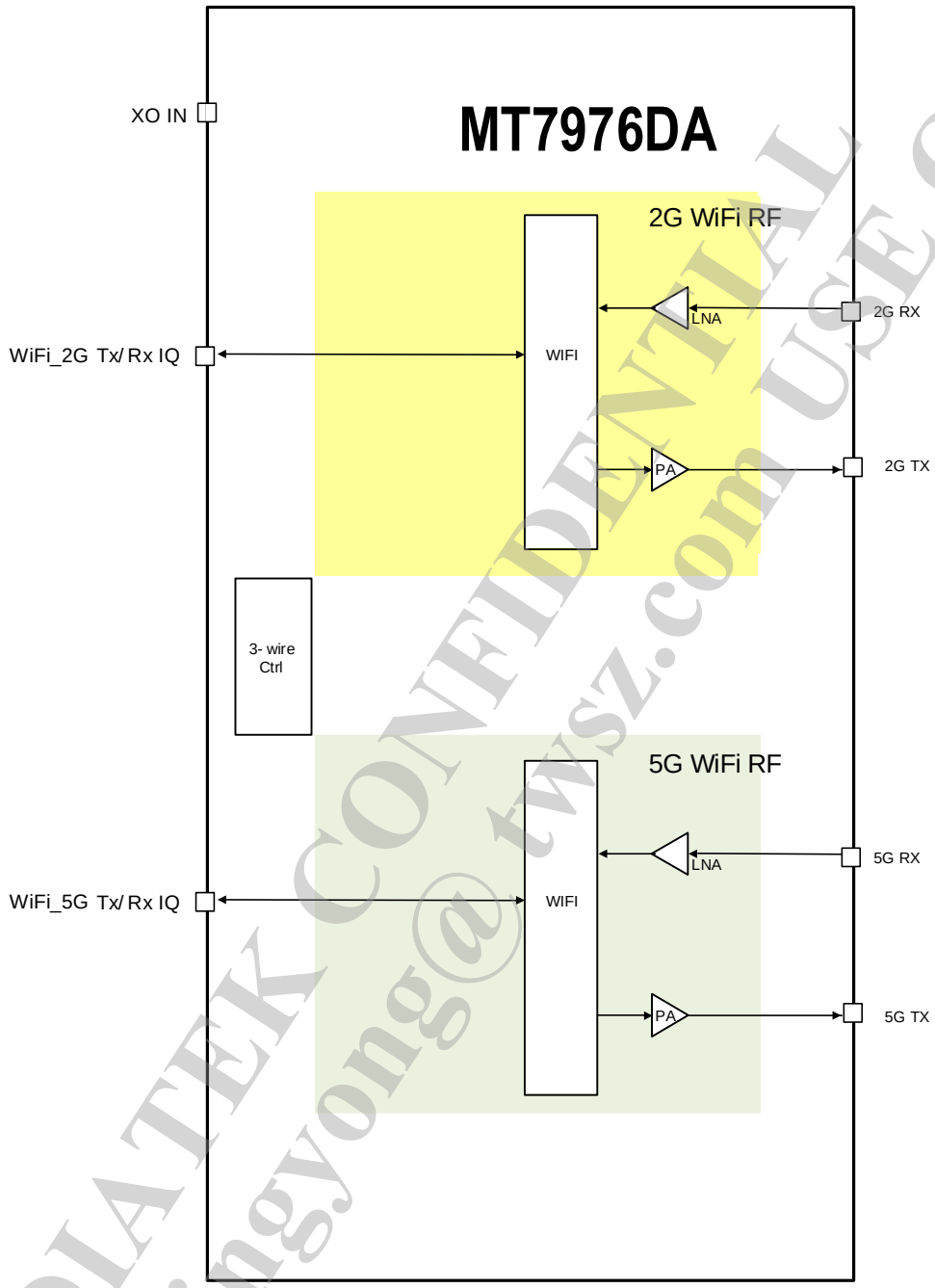


Figure 1-1. MT7976DAN block diagram

1.2 Features

- MT7976DAN is an IEEE WiFi 6 MIMO RF chip which contains 2.4 GHz WI-Fi transceiver front-ends and 5 GHz Wi-Fi transceiver front-ends in a DRQFN package.

1.2.1 Wi-Fi Transceiver

WLAN

- Dual-band (2.4GHz and 5/6GHz) MIMO 802.11 a/b/g/n/ac/ax RF, 20/40/80/160MHz bandwidth
- Built-in calibrations for PVT variation
- Supports external PA and LNA for WiFi-2.4GHz and WiFi-5/6GHz.

2 Pin Definitions (draft)

2.1 Pin Layout

MT7976DAN uses DRQFN package of with 12.5mm x 10mm dimension.

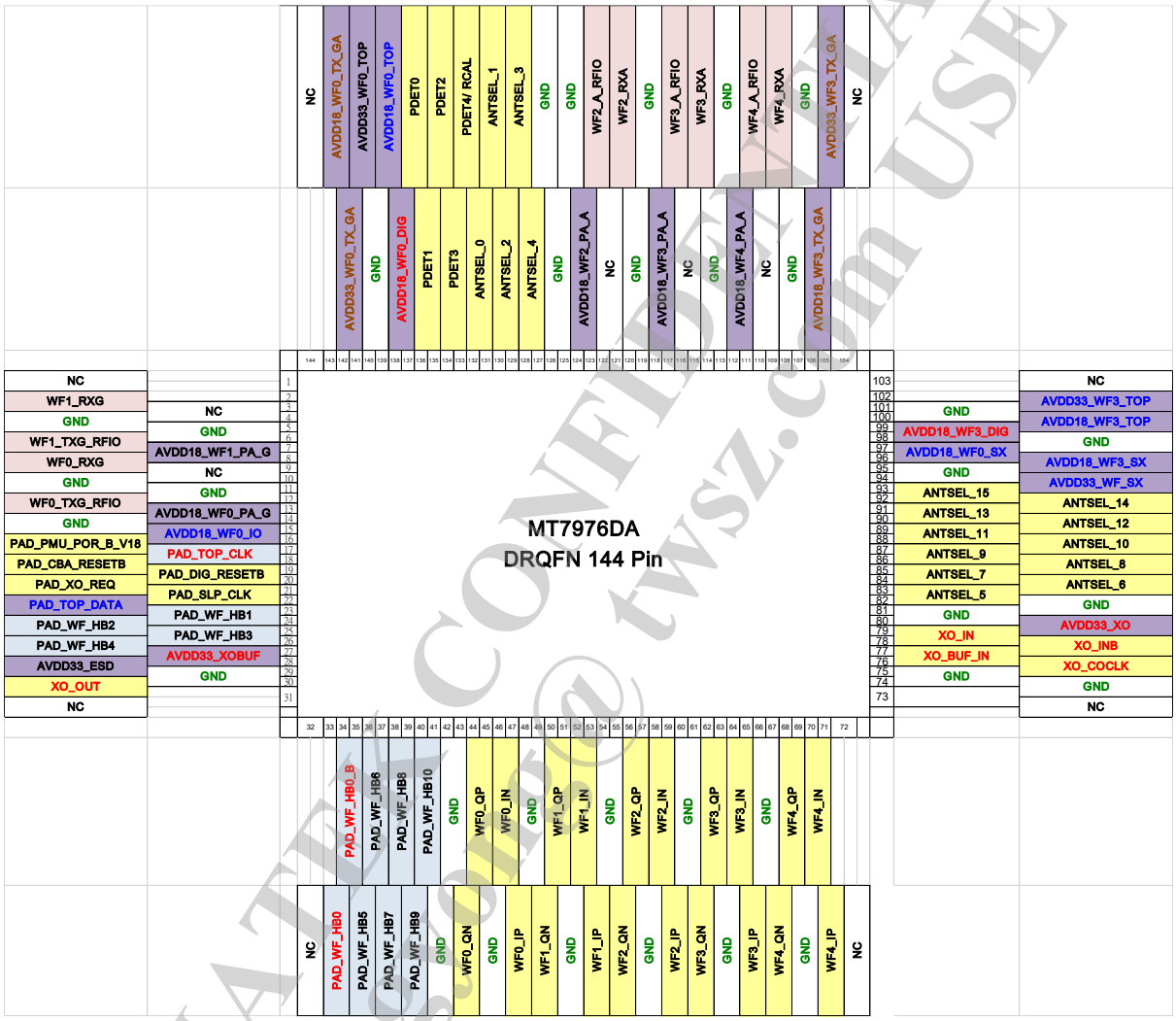


Figure 2-1. MT7976DAN pin definition

2.2 IO Definitions

The IO definitions used in Table 2-1 are listed below.

Table 2-1. I/O definitions

Pad attribute	
AI	Analog input (excluding pad circuitry)
AO	Analog output (excluding pad circuitry)
AIO	Analog bidirectional (excluding pad circuitry)
DIO	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
Z	High-impedance (high-Z) output
NP	No internal pull
PU	Internal pull-high
PD	Internal pull-low
ADIO	Analog and digital IO (excluding pad circuitry)
Power	Voltage supply
GND	Ground
NC	No connection

2.3 Pin Definitions

Details pin descriptions of MT7976DAN are listed in the following table.

DRQFN	Pin Name	Pin description	PU/PD	I/O	Supply domain
GND pins					
4,5,10,11, 14,29,41,42, 45,48,51,54, 57,60,63,66, 69,74,75,81, 82,95,98,101, 107,108, 113,114, 119,120, 125,126, 127,140	GND	GND	N/A	GND	
1,3,9,31, 32,72,73,103, 104,110,116, 122,144	NC	NC	N/A	NC	
79	XO_IN	Crystal positive input	N/A	AI	
78	XO_INB	Crystal negative input	N/A	AI	
77	XO_BUF_IN	external clock input	N/A	AI	
80	AVDD33_XO	XO 3.3v power supply	N/A	Power	
27	AVDD33_XOBUF	XO 3.3v power supply	N/A	Power	
76	XO_COCLK	XTAL buffered clock output	N/A	AO	
30	XO_OUT	XTAL buffered clock output	N/A	AO	
WIFI Power supply					
13	AVDD18_WF0_PA_G	RF 1.8v power supply	N/A	Power	
7	AVDD18_WF1_PA_G	RF 1.8v power supply	N/A	Power	
143	AVDD18_WF0_TX_GA	RF 1.8v power supply	N/A	Power	
142	AVDD33_WF0_TX_GA	RF 3.3v power supply	N/A	Power	
124	AVDD18_WF2_PA_A	RF 1.8v power supply	N/A	Power	
118	AVDD18_WF3_PA_A	RF 1.8v power supply	N/A	Power	
112	AVDD18_WF4_PA_A	RF 1.8v power supply	N/A	Power	
106	AVDD18_WF3_TX_GA	RF 1.8v power supply	N/A	Power	
105	AVDD33_WF3_TX_GA	RF 3.3v power supply	N/A	Power	
141	AVDD33_WF0_TOP	RF 3.3v power supply	N/A	Power	

138	AVDD18_WF0_DIG	RF 1.8v power supply	N/A	Power	
139	AVDD18_WF0_TOP	RF 1.8v power supply	N/A	Power	
99	AVDD18_WF3_DIG	RF 1.8v power supply	N/A	Power	
100	AVDD18_WF3_TOP	RF 1.8v power supply	N/A	Power	
102	AVDD33_WF3_TOP	RF 3.3v power supply	N/A	Power	
97	AVDD18_WF0_SX	RF 1.8v power supply	N/A	Power	
96	AVDD18_WF3_SX	RF 1.8v power supply	N/A	Power	
94	AVDD33_WF_SX	RF 3.3v power supply	N/A	Power	
15	AVDD18_WF0_IO	RF 1.8v power supply	N/A	Power	
28	AVDD33_ESD	RF 3.3v power supply	N/A	Power	
WIFI Radio Frequency interface					
137	PDET0	External TSSI DC input	N/A	AI	
136	PDET1	External TSSI DC input	N/A	AI	
135	PDET2	External TSSI DC input	N/A	AI	
134	PDET3	External TSSI DC input	N/A	AI	
133	PDET4	External TSSI DC input			
123	WF2_A_RFIO	RF A-band RF port	N/A	AIO	
117	WF3_A_RFIO	RF A-band RF port	N/A	AIO	
111	WF4_A_RFIO	RF A-band RF port	N/A	AIO	
6	WF1_TXG_RFIO	RF G-band RF port	N/A	AIO	
12	WF0_TXG_RFIO	RF G-band RF port	N/A	AIO	
8	WF0_RXG	G-band External LNA input	N/A	AI	
2	WF1_RXG	G-band External LNA input	N/A	AI	
121	WF2_RXA	A-band External LNA input	N/A	AI	
115	WF3_RXA	A-band External LNA input	N/A	AI	
109	WF4_RXA	A-band External LNA input	N/A	AI	
WIFI Analog interface					
47	WF0_IP	WF0 IF TRX IQ signals	N/A	AIO	
46	WF0_IN	WF0 IF TRX IQ signals	N/A	AIO	
44	WF0_QP	WF0 IF TRX IQ signals	N/A	AIO	
43	WF0_QN	WF0 IF TRX IQ signals	N/A	AIO	
53	WF1_IP	WF1 IF TRX IQ signals	N/A	AIO	
52	WF1_IN	WF1 IF TRX IQ signals	N/A	AIO	
50	WF1_QP	WF1 IF TRX IQ signals	N/A	AIO	
49	WF1_QN	WF1 IF TRX IQ signals	N/A	AIO	
59	WF2_IP	WF2 IF TRX IQ signals	N/A	AIO	
58	WF2_IN	WF2 IF TRX IQ signals	N/A	AIO	

56	WF2_QP	WF2 IF TRX IQ signals	N/A	AIO	
55	WF2_QN	WF2 IF TRX IQ signals	N/A	AIO	
65	WF3_IP	WF3 IF TRX IQ signals	N/A	AIO	
64	WF3_IN	WF3 IF TRX IQ signals	N/A	AIO	
62	WF3_QP	WF3 IF TRX IQ signals	N/A	AIO	
61	WF3_QN	WF3 IF TRX IQ signals	N/A	AIO	
71	WF4_IP	WF4 IF TRX IQ signals	N/A	AIO	
70	WF4_IN	WF4 IF TRX IQ signals	N/A	AIO	
68	WF4_QP	WF4 IF TRX IQ signals	N/A	AIO	
67	WF4_QN	WF4 IF TRX IQ signals	N/A	AIO	
Digital IOs					
19	PAD_DIG_RESETB	Hardware reset from companion modem	PU/PD	DI	DVDDIO
18	PAD_CBA_RESETB	software reset from companion modem	PU/PD	DI	DVDDIO
20	PAD_XO_REQ	XO enable control from companion modem	PU/PD	DI	DVDDIO
21	PAD_SLP_CLK	Sleep CLK input/output	PU/PD	DIO	DVDDIO
22	PAD_TOP_DATA	TOP 2-wire data signal	PU/PD	DIO	DVDDIO
17	PAD_TOP_CLK	TOP 2-wire clock signal	PU/PD	DI	DVDDIO
40	PAD_WF_HB10	WF high speed control bus	PU/PD	DIO	DVDDIO
39	PAD_WF_HB9	WF high speed control bus	PU/PD	DIO	DVDDIO
38	PAD_WF_HB8	WF high speed control bus	PU/PD	DIO	DVDDIO
37	PAD_WF_HB7	WF high speed control bus	PU/PD	DIO	DVDDIO
36	PAD_WF_HB6	WF high speed control bus	PU/PD	DIO	DVDDIO
35	PAD_WF_HB5	WF high speed control bus	PU/PD	DIO	DVDDIO
26	PAD_WF_HB4	WF high speed control bus	PU/PD	DIO	DVDDIO
25	PAD_WF_HB3	WF high speed control bus	PU/PD	DIO	DVDDIO
24	PAD_WF_HB2	WF high speed control bus	PU/PD	DIO	DVDDIO
23	PAD_WF_HB1	WF high speed control bus	PU/PD	DIO	DVDDIO
34	PAD_WF_HB0_B	WF high speed control bus	PU/PD	DIO	DVDDIO
33	PAD_WF_HB0	WF high speed control bus	PU/PD	DIO	DVDDIO
16	PAD_PMU_POR_B_V18	Chip enable from companion modem	PU/PD	DI	DVDDIO
FEM IOs					
83	ANTSEL_5	FEM control	PU/PD	DIO	DVDDIO
84	ANTSEL_6	FEM control	PU/PD	DIO	DVDDIO
85	ANTSEL_7	FEM control	PU/PD	DIO	DVDDIO
86	ANTSEL_8	FEM control	PU/PD	DIO	DVDDIO
87	ANTSEL_9	FEM control	PU/PD	DIO	DVDDIO

88	ANTSEL_10	FEM control	PU/PD	DIO	DVDDIO
89	ANTSEL_11	FEM control	PU/PD	DIO	DVDDIO
90	ANTSEL_12	FEM control	PU/PD	DIO	DVDDIO
91	ANTSEL_13	FEM control	PU/PD	DIO	DVDDIO
92	ANTSEL_14	FEM control	PU/PD	DIO	DVDDIO
93	ANTSEL_15	FEM control	PU/PD	DIO	DVDDIO
128	ANTSEL_4	FEM control	PU/PD	DIO	DVDDIO
129	ANTSEL_3	FEM control	PU/PD	DIO	DVDDIO
130	ANTSEL_2	FEM control	PU/PD	DIO	DVDDIO
131	ANTSEL_1	FEM control	PU/PD	DIO	DVDDIO
132	ANTSEL_0	FEM control	PU/PD	DIO	DVDDIO

Table 2-2 MT7976DAN common pin descriptions

3 Electrical Characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.6	V
VDD18	1.8V Supply Voltage	-0.3 to 1.89	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V
VESD	ESD protection (CDM)	+/- 250	V

Table 3-1 Absolute maximum rating

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	3	3.3	3.6	V
VDD18	1.8V Supply voltage	1.71	1.8	1.89	V
$T_{JUNCTION}$	Industry junction operating temperature	-20	25	125	°C
$T_{AMBIENT}$	Ambient Temperature	-10	-	70	°C

Table 3-2 Recommended operating range

3.3 Power Supply Specifications

The following tables list the power supply requirements for VDD18 and VDD33.

Table 3-3. AVDD18 specifications

Test item	Min.	Typ.	Max.	Unit	Notes
Output voltage, VDD	1.71	1.8	1.89	V	
Output current				mA	

Table 3-4. AVDD33 specifications

Test Item	Min	Typ	Max	Unit	Notes
Output voltage	3.0	3.3	3.6	V	
Output current				mA	

3.4 Digital Logic Characteristics

MT7976DAN’s timing characteristics and interface protocols are shown here, including some general comments.

3.4.1 Timing Diagram Convention

Figure 3-1 shows the conventions used with timing diagram throughout this document.

Waveform	Description
	Signal is changing from low to high
	Signal is changing from high to low
X	Don’t care or bus is driven
	Bus is changing from invalid to valid
	Bus is changing from high-Z to valid
	Denotes multiple clock periods

Figure 3-1. Timing diagram conventions

3.4.2 Rising/Falling Time Definition

Figure 3-2 is the rising and falling timing diagram. The actual signal timing curve is related to the external load conditions. See **錯誤! 找不到參照來源。** for the operating conditions of digital logics.

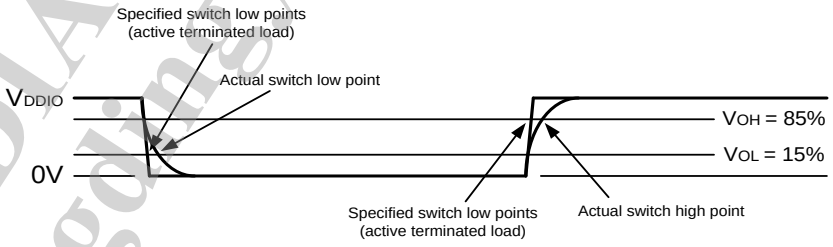


Figure 3-2. Rising and falling times diagram

Table 3-5. Operating conditions of digital logics

Parameter	Min.	Typ.	Max.	Unit	Notes
VDDIO, supply of IO Power	3	3.3	3.6	V	
VIH, input logic high voltage	0.7*VDD		VDD+0.5	V	
VIL, input logic low voltage			0.3*VDDIO	V	
VOH (DC), DC output high voltage	0.7*VDD		VDD+0.5	V	VDD=min, I_{OH}=1.5mA
VOL (DC), DC output low voltage			0.3*VDD	V	VDD=min, I_{OL}=1.5mA

3.4.3 Protocols

There are three main interfaces for MT7976DAN:

- 2-wire top control interface: Generally used for all systems (Wi-Fi)
- 12-wire bus: High-speed interface, for Wi-Fi

3.4.3.1 2-Wire

The 2-wire bus of MT7976DAN is mainly used as below:

- Top control interface, the main interface to access Wi-Fi/TOP command registers

The bit number of SDATA depends on different operating conditions, as shown in Figure 3-3.

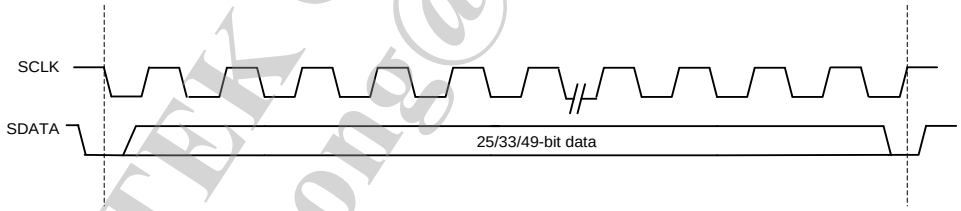


Figure 3-3. 2-wire SPI timing diagram

3.4.3.2 9-bit Bus

MT7976DAN has a dedicated 9-bit bus to control the Wi-Fi radio. The related control definitions depend on operating modes and conditions. The protocol is shown in Figure 3-4.

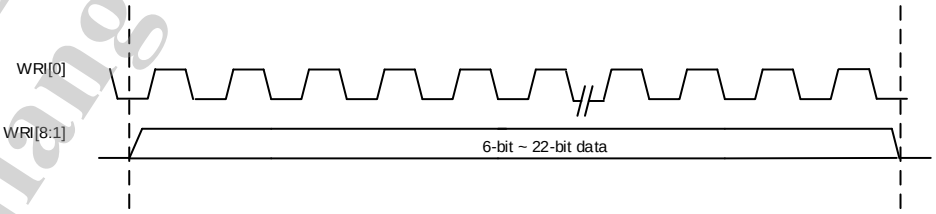


Figure 3-4. Wi-Fi 9-wire SPI access

3.5 MT7976DAN TOP Building Blocks

3.5.1 Thermal ADC

A low-speed ADC converts the output of thermal sensor. The temperature coverage range is between -40˚C and 120˚C. The chip top control may do corresponding adjustment based on such temperature information.

3.6 Wi-Fi

MT7976DAN Wi-Fi is a high performance and highly-integrated dual-band RF transceiver fully compliant with IEEE 802.11 a/ac/ax/b/g/n standards. MT7976DAN features a self-calibration scheme to compensate the process and temperature variation to maintain high performance. The calibration is performed automatically right after the system boot-up.

3.6.1 2.4GHz Wi-Fi Tx

The 2.4GHz transmitter integrates a PA Driver with on-chip balun. The data are digitally modulated in the baseband processor from the companion chip, then up-converted to 2.4GHz RF channels through the DA converter, filter, IQ up-converter and PA Driver.

3.6.2 2.4GHz Wi-Fi Rx

The 2.4GHz Wi-Fi Rx consists of a high linearity, low noise figure single-ended LNA, a quadrature passive mixer and a bandwidth-programmable low-pass filter with DC offset cancellation embedded.

3.6.3 2.4GHz Wi-Fi Sx

A fractional-N frequency synthesizer is implemented to support Wi-Fi LO signal. The frequency synthesizer is capable of supporting various crystal clock frequencies. VCO operates at different freq from RF frequency to avoid any coupling with RF front-end circuitry. An LO generation is employed to divide the VCO signal and generate I/Q quadrature signals.

3.6.4 5/6GHz Wi-Fi Tx

The 5/6GHz transmitter integrates a high performance PA Driver with on-chip balun. The data are digitally modulated in the baseband processor from the companion baseband chip, then up-converted to 5/6GHz RF channels through the DA converter, low-pass filter, IQ up-converter and PA Driver

3.6.5 5/6GHz Wi-Fi Rx

The 5/6GHz Wi-Fi Rx consists of a high linearity, low noise figure single-ended LNA, a quadrature passive mixer and a bandwidth-programmable low-pass filter with DC offset cancellation embedded.

3.6.6 5/6GHz Wi-Fi Sx

A-band Sx adopts LO architecture while VCO frequency is different from RF frequency to avoid TX pulling. Thus, it is composed of PLL, offset LO mixer and a repeater.

4 XO and Bootstrap

4.1 XTAL oscillator

The table below lists the requirement for the XTAL.

Item	Spec.
Nominal Frequency	40MHz
Size	3.2mmx2.5mm
Operating Temperature Range	-40°C to +105°C
Frequency Tolerance (FL)	+/- 7 ppm @ 25°C +/- 3°C
Frequency Stability over Operating Temperature	+/- 15 ppm (referred to the value at 25°C) -40°C to +100°C +/- 20 ppm (referred to the value at 25°C) 100°C to +105°C
Equivalent Series Resistance (ESR)	15 Ω max.
Drive Level(DL)	400uW max
Shunt Capacitance (Co)	3.0 pF max
Load Capacitance (CL)	10 pF
Trim Sensitivity Over Load(Ts)	10~13 ppm/pF

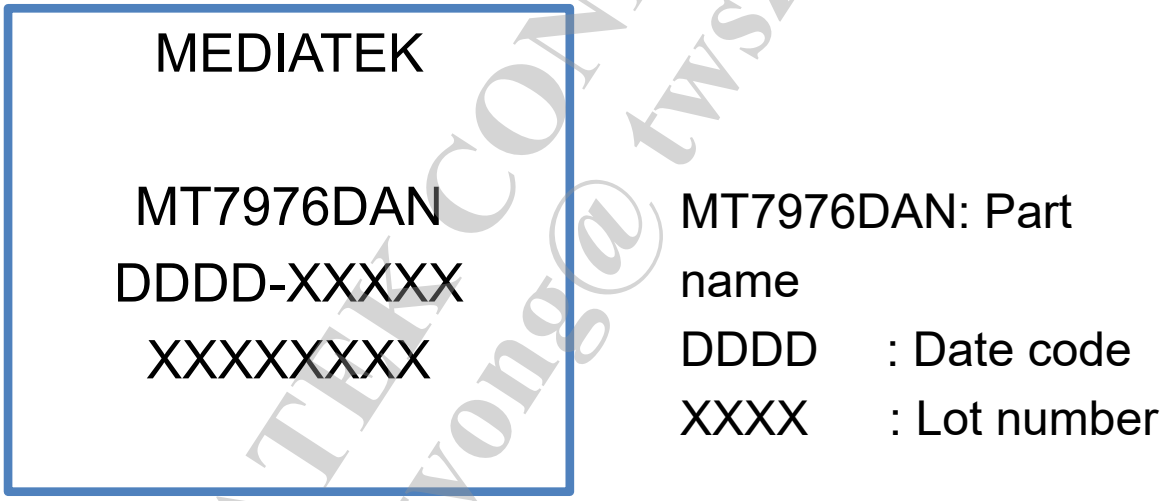
Table 4-1 XTAL oscillator requirement

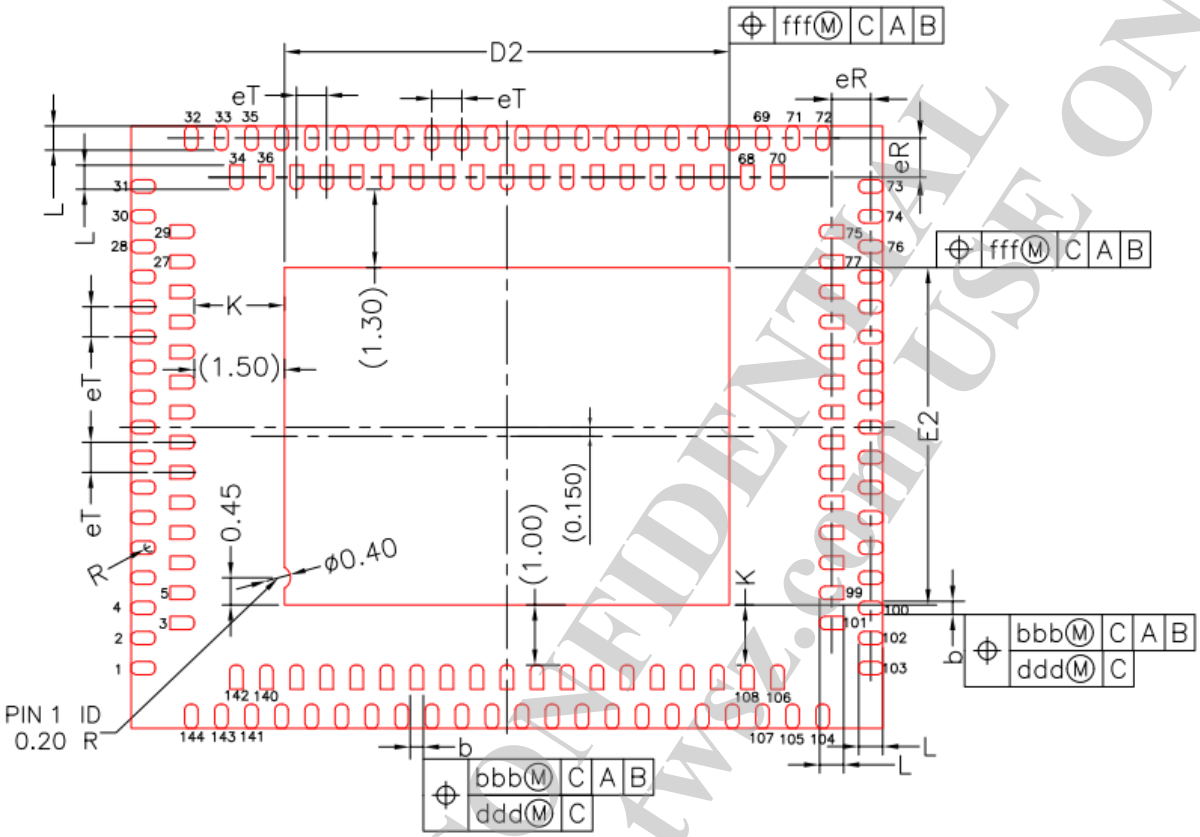
5 Mechanical Information

5.1 Device Physical Dimension/Part Number

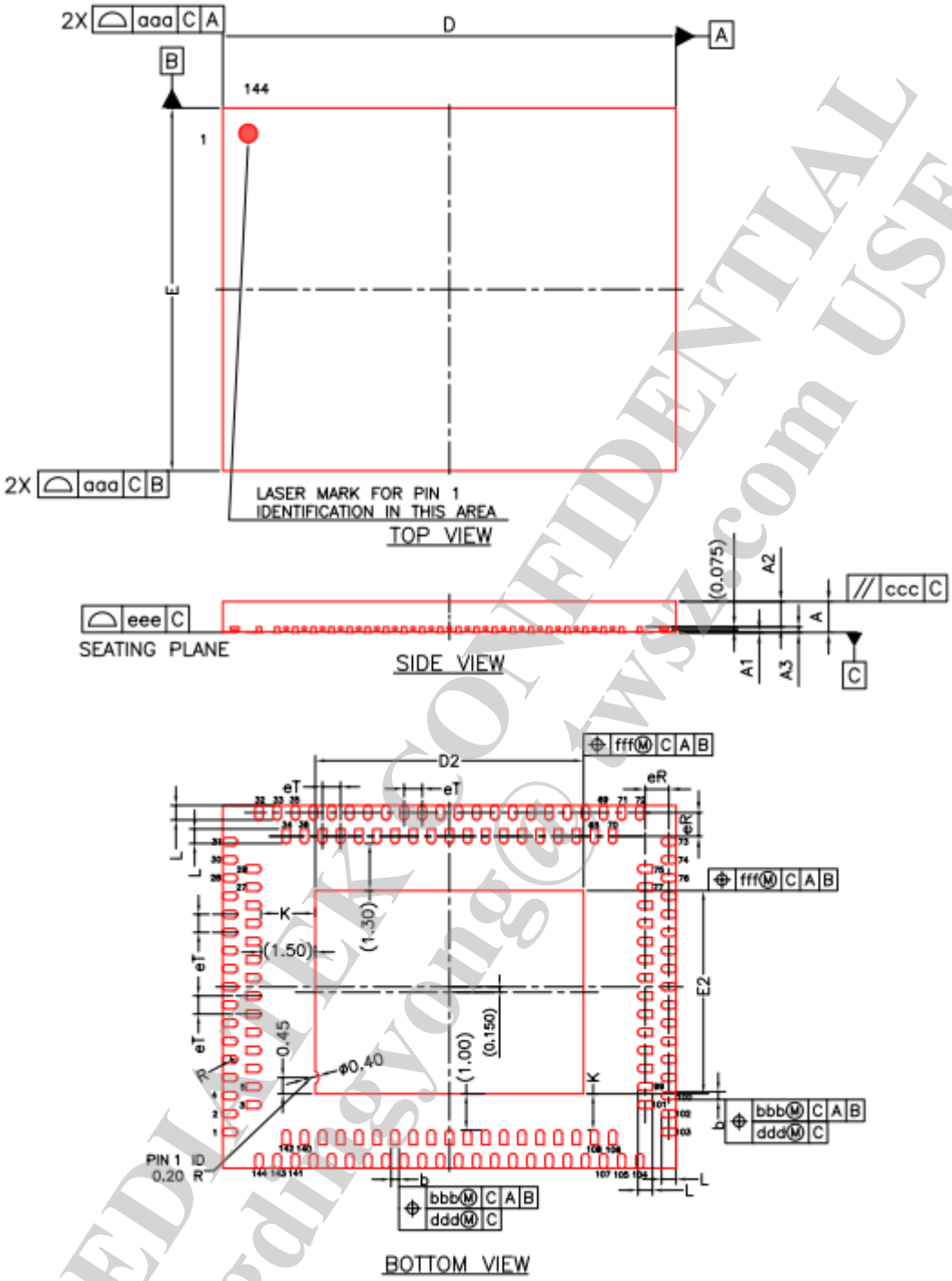
MT7976DAN uses DRQFN package. The physical dimension is shown in Figure 5-1.

Figure 5-1. Physical dimension of MT7976DAN





Bottom View



Item		Symbol	MIN.	NOM.	MAX.
Total height		A	0.80	0.85	0.90
Stand off		A1	0.00	0.02	0.05
Mold thickness		A2	0.65	0.70	0.75
Lead frame thickness		A3		0.15 REF.	
Lead width		b	0.18	0.22	0.30
Package size	X	D	12.40	12.50	12.60
	Y	E	9.90	10.00	10.10
E-PAD size	X	D2	7.30	7.40	7.50
	Y	E2	5.50	5.60	5.70
Lead length		L	0.30	0.40	0.50
Lead pitch		eT		0.50 bsc	
Lead pitch		eR		0.65 bsc	
Lead arc		R	0.090	---	0.140
Lead to E-PAD tolerance		K	0.80	---	---
Package tolerance		aaa		0.10	
Package profile of a surface		bbb		0.10	
Lead profile of a surface		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

TITLE			
PACKAGE OUTLINE 144 L DR-SQFN 12.5X10 X 0.9 mm		MEDIATEK	
DWG. NO.	REV.	SHEET	UNIT
MT-AP01502	A	1 OF 2	MM

Figure 5-2. Physical dimension of MT7976DAN

5.2 Ordering Information

Order No.	Marking	Temperature range	Package
MT7976DAN	MT7976DAN	-10°C ~ 70°C	DRQFN

ESD CAUTION

MT7976DAN is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7976DAN is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.