i.MX51 Generic Reference Design

Freescale Semiconductor Confidential

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ICAP Classification: FCP: __ FIUO: X PUBI: __

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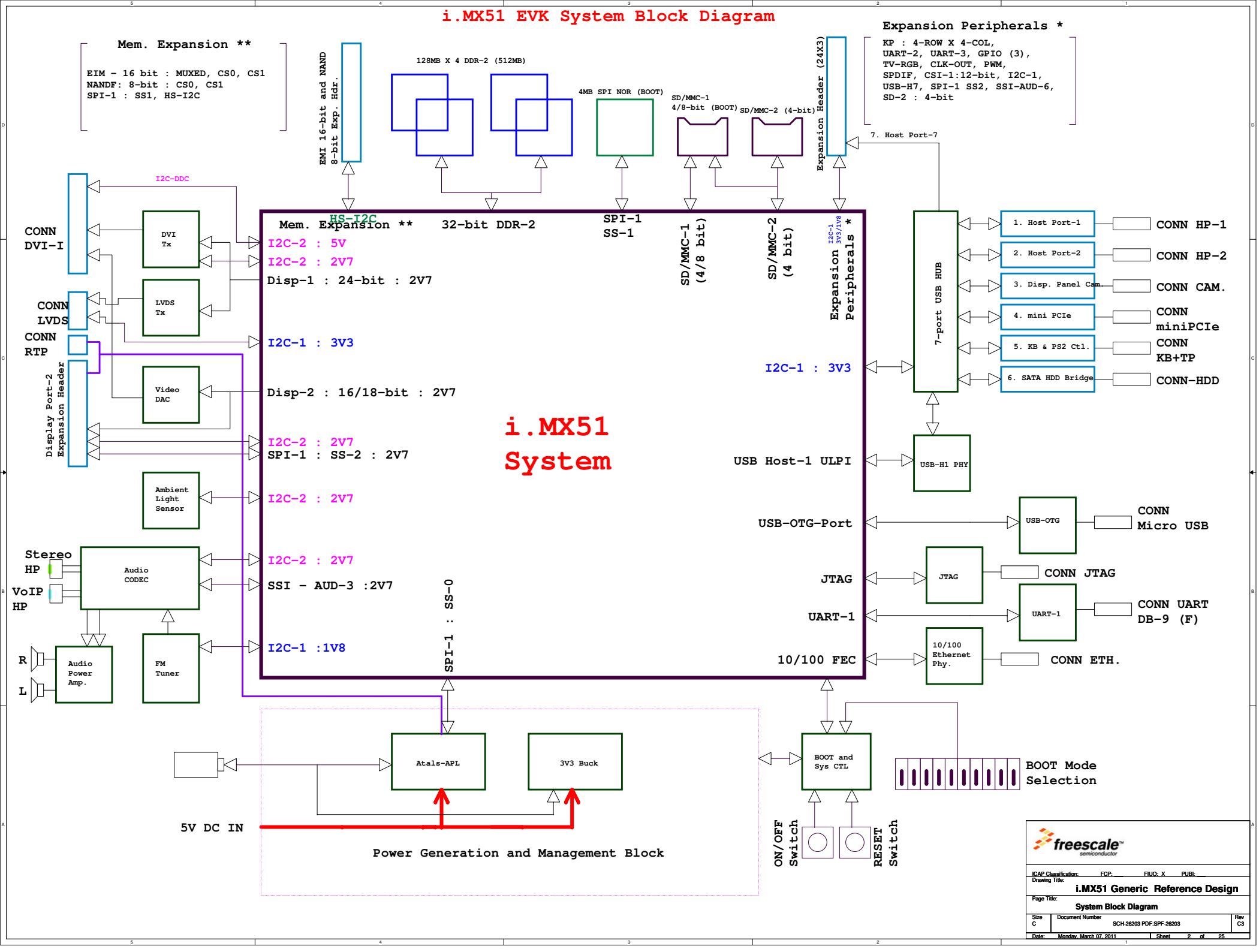
i.MX51 EVK System Block Diagram



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Programmers Notes

1. Since IPU_Port_2 has two loads (DVI and LVDS), this may require a different (higher) drive strength setting than IPU_Port_2

I2C Port Summary

MX51 Port	Voltage Rail	Device	Primary Address	Secondary Address	Comment
I2C1	1.8	FM Radio	0010000x		
I2C1	1.8	Expansion Connector	---		Level converted
I2C1	3.3	Expansion Connector	---		Level converted
I2C1	3.3	USB Hub (option)			Level converted
I2C1	3.3	LVDS Connector			Level converted
I2C2	2.775	Audio CODEC	0001010x		
I2C2	2.775	DVI Chip	1110010x	1110110x	
I2C2	2.775	Parallel Dumb Display Connector			
I2C2	2.775	Ambient Light Sensor	1000100x		
I2C2	5	DVI Connector	0110111x	0101000x	Level converted

Daily change report

April 20
(1) change the R246 to DNP for Audio function
April 22
(1) change the R20 value to 120K
(2) Change the C53 tolerance to 10V
(3) Change the R243 Q17 R85 and C81 DNP
(4) Add the missing GND net of the U234
(5) change the RN2 and RN3 to MNR15E0RPJ103;change the RN4 toMNR15E0RPJ102
(6) change the PAD1---PAD5 to 0ohm 0805 resistor
April 24
(1) change the J12 manufacture NO. to FH12-26S-1SH(55). 1mm pitch connector for Keypad
(2) Change the Y5 to DNP
(3) Change J3 to through hole 1x4 2.54 pitch connector
(4) Change the R397 and R398 to DNP
(5) Change the R277 and R279 to DNP. And R285 should be installed.
(6) Change the U44A,L31-L39,C345-C360,R265-R268,D30-D34 to DNP to disable the VGA function
(7) DNP the U4,Q1-Q4,D6,D7,D9,D10,L1,J2,R14-R28,R30,R31,R33-R35 and c4-c31 to disable the battery charger function
(8) Change the R60 value to 13.7K
(9) Change the R58 value to 33K
April 27
(1) change the value of R58 to 38.3K
(2) DNP J3
(3) DNP L22
April 28
(1) change C68 to 150-77976 10V tolerance
(2) C73 change back to 150-75182
(3) C47,C48 change back to 150-75837
(4) Populate R72 and R76, DNP R71 and R75
(5) change R11, R179 to 470-75597
(6) Change the value of R170 to 33ohm
(7) Change the value of R365-R372 to 1Kohm
(8) Change R341 to 470-75591
(9) Change R314 and R315's footprint to 0402
(10) change C243,C245,C248,C251 to T491C107K016ZT, 100uF/16V
(11) change Y1 to 230-77492
(12) change Y3 to 230-77493, change the C250 and C253 to 15pF
(13) change Y6 to 230-77493, change the C384 and C385 to 15pF, change R333 to 1.0M
(14) change Y5 to 230-77047
(15) change Y2 to 230-77698
(16) change Y4 and Y7 to 230-76393, change C301, C302, C420 and C421 to 10pF
(17) C42,C43,C51,C52 need to be Panasonic T520B157M006ATE045 (Low ESR)
(18) change L40,L45,L46 to be 3000hm@100MHz FB
April 29
(1) change C410 footprint to 0402
(2) Correct the connection of the J9
(3) Change J5 to 5622-1200-ML
May 4
(1) change U41A and U44A to U41 and U44
(2) Swap the connection of the J16 to be compatible with SGTL Nand board
(3) C2 is too large in value. Time delay too big for power-off. Change C2 to 22uF 20V.
(4) put 0-ohm series resistor on DDC-SCL and DDC_SDA lines (0402) R1002 and R1003
May 6
(1) change Y3 back to ECS part,change C250 and C253 back to 33pF
(2) Change the net name PWR_ON_OFF_BYPASS2 to PWR_ON_OFF_BYPASS
(3) As Babin David comment, DNP D11 and D14
(4) Add R1004 a series zero-ohm on VREG and DNP
(5) Correct the connection of the Y2
(6) Swape the R474 and R476, also R292 and R270
(7) change the DDR2 chips to EDE1116AEBG-8E-F to support 800Mhz
May 7
(1) change D11,D14 and D24 to fairchild LED part QTLP600CBTR
(2) Adjust the connecton of J18, add the backlight of the AAPL
May 11
(1) Add Pad6 and Pad7 to support the external 5V power supply
(2) Use DI_GP1 and DI_GP2 as LCD interrupt and LP mode
May 12
(1) Add R1011 and R1012, the series resistors on I2C of U234
(2) populated the C337
(3) change R1 and R3 to diode
May 13
(1) Delete D8, add Q2001 P-FET for reverse polarity protection.
(2) Delete the MAX8505 and other peripheral components
(3) Change R58 to 33.2K/1% to make TPS51124 LX1 output 3.3V
(4) Update the power supply circuit for AAPL
(5) Add R3002 and R3003 to make the PMIC_STBY_REQ signal alternatively
(6) Change the value C250 and C253 to 15pF
(7) update the connection of the display connector
(8) Add 330pF capacitors to GND of DVI I2C
(9) Update the connection of the Expansion connector
May 14
(1) Move R98 and R99 to I2C master
(2) correct GND nets throughout the entire design
(3) U11, U12, U13 should all be eliminated from the board. We do not need the SST part
May 15
(1) Change U14 to 4MB Flash
May18
(1) SD_MMC_CD_B move to GPIO1_6. New net name is SD_MMC_CD_B(GPIO1_6).WDOG_B move to GPIO1_4. New name is WDOG_B(GPIO1_4).
DISP_CARD_DET_B move to DI1_PIN13. (This is new signal for i.MX51 EVK RevB) New name is DISP_CARD_DET_B(DI1_PIN13_GPIO3_2).
(2) Add 5V_MAIN control circuit
May 20
(1) Delete TPS51124, add the Linear 3.3V buck LT3681
May 21
(1) Change the 3V3 regulator
(2) U7 pin K9 to J14 pin 83 with 10K 1% pullup to 3V15_BOOT Net name = "ACCESSORY_CARD_ID0"
U7 pin M11 to J14 pin 61 with 10K 1% pullup to 3V15_BOOT Net name = "ACCESSORY_CARD_ID1"
use R69, R68 for 10K 1% resistors. delete R73.
(3) Delete GPO1\SPI1_SS2_DISP_HDR_EN_B\SPI1_SS2_EXP_HDR_EN_B\3V3_V5A_PWRGD\BATT_IN(GPIO1_22)
May 25
(1) Add the R5019
(2) Change the part number of the H1 to H4
(3) Add DISP2_RESET net, change net ACCESSORY_CARD_DETECT_B to GPIO4_13
(4) Change Q2002 to Q2004 to make sure the power dissipation enough
(5) pull up WDOG_B(GPIO1_4) to 2V775_BOOT and DNP R89
(6) DNP R423,R424,R425 and R428
(7) Populate the R132
(8) Change R146 and R147 to 1K 0.5% precision
May 27
(1) Add R6001 the pull down resistor
(2) update the connection of J14
(3) Change R250 pull up to V_SPKR
Jun 2
(1) change a larger MOSFET for Q2001
(2) Delete R131
(3) Change H1-H4 DNP
(4) DNP Keyboard page, FM receiver page and light sensor moduler
(5) Update the Sw1 and Sw4 circuit design of AAPL, change to P-FET
(6) Change the C3001 to 10uF
June 3
(1) Populate CON1
(2) J14 pin 52... connect to pin 61. PORT_ID1
(3) Change another part for Q2002-Q2004
(4) Add D7001,D7002,R7001 and R7002
June 4
(1) DNP R337
June 5
(1) Populate Q5001 and DNP R5010
(2) Change R146 and R147 to 1K 1% precision
June 11
(1) Change the Y2 P/N, 2.775V power supply
(2) Add the Analog Devices RGB circuit back into the board
(3) Change DVI_i2C bypass capactiors to 220pF
July 13
(1) Change R3001 value to 0.02ohm
(2) Connect Atlas pin D8 to GND
(3) DNP L1001
(4) Populate R5010, DNP R5009,Q5001,U5002
(5) Populate R89
(6) DNP R68
(7) Add R8001 100K resistor in parallel with C70
(8) Disconnect ADIN5 from Card-detect. Tie it to 10K/10K
resistor divider to GP01 of Atlas (i.MX51 EVK RevB tie directly to
VCOREDIG)
(9) R332 change to 2.2K ,R329 change to 2.2K, DNP
(10) Change the JTAG part number
(11) Change R1001 and R1002 to FB8001 and FB8002
(12) Populate R399 and R400
(13) Add GPIO4_14 to control DVI I2C level shifter and DNP 220pF capacitor
(14) Change Y2 and Y6 part
(15) Update the Y5 part
July 28
(1) Change R146 and R147 to 768ohm 1%
Aug 04
(1) Populate Y5
Aug 10
(1) DNP R491 and R492
Aug 27
(1) Cut the DVI_I2C path, DNP FB8001 and FB8002
Sep 3
(1) Change the AAPL to ITC part
(2) Change the MX51 to ITC part
(3) reverse the polarity of the capacitors of C339 and C341

i.MX51EVKJ change list:
Nov 11
(1) Change R7001 and R7002 to 47K to reduce power dissipation
(2) Add RE001 connect GND_ENET to GND
(3) Add RA001 and RA002, provide a 4.2V voltage to VBAT for AAPL
(4) Delete H5 and H6, make them as vias in PCB
(5) Connect USB_5V to 5V_IN
(6) change U33 to TI part and populate the DVI_I2C path back
(7) Add net 3V3_PWEN to control 3V3 power with GPIO4_15
(8) change R79,R82,R84-R87(0.02ohm) connectiong, make sure the power path can be cut by removing the resistors

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Page Title: **Notes for Programmers and Layout**

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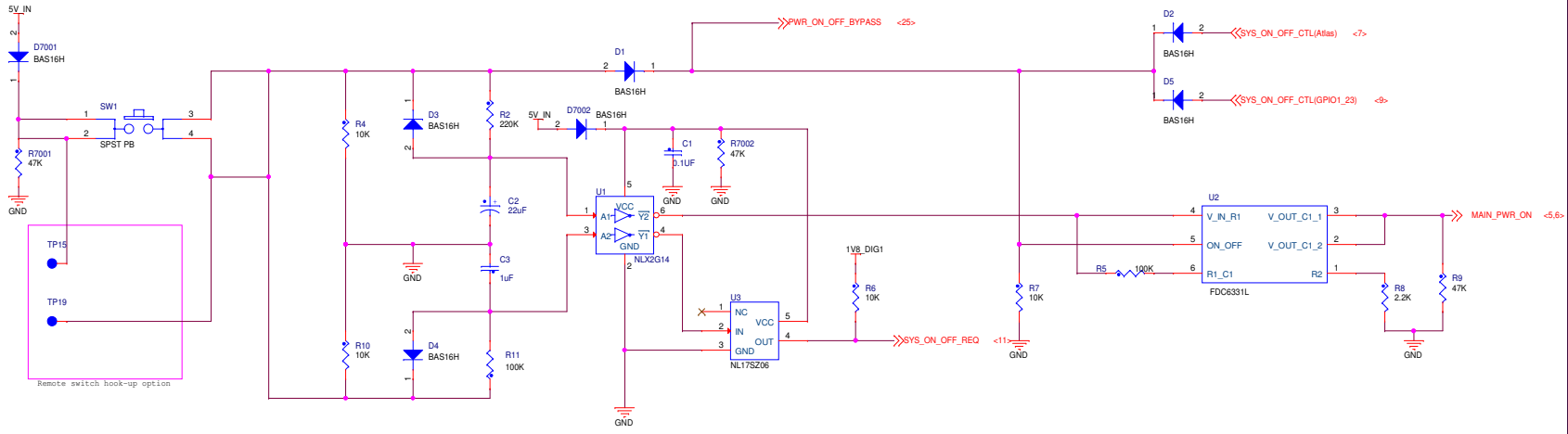
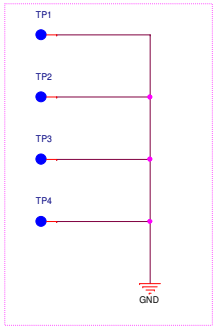


If system is OFF,
press momentary contact switch to turn system ON.

If system is ON,
press momentary contact switch to start s/w based
shutdown_entry or resume operation.

If system is hung, press contact switch for at least 10 seconds.



TP1 and TP2 on top.
TP3 and TP4 on bottom.

Silk screen label as GND.

Note:
To increase or decrease the forced turn-off time, change RC timing by changing R2 and C2.

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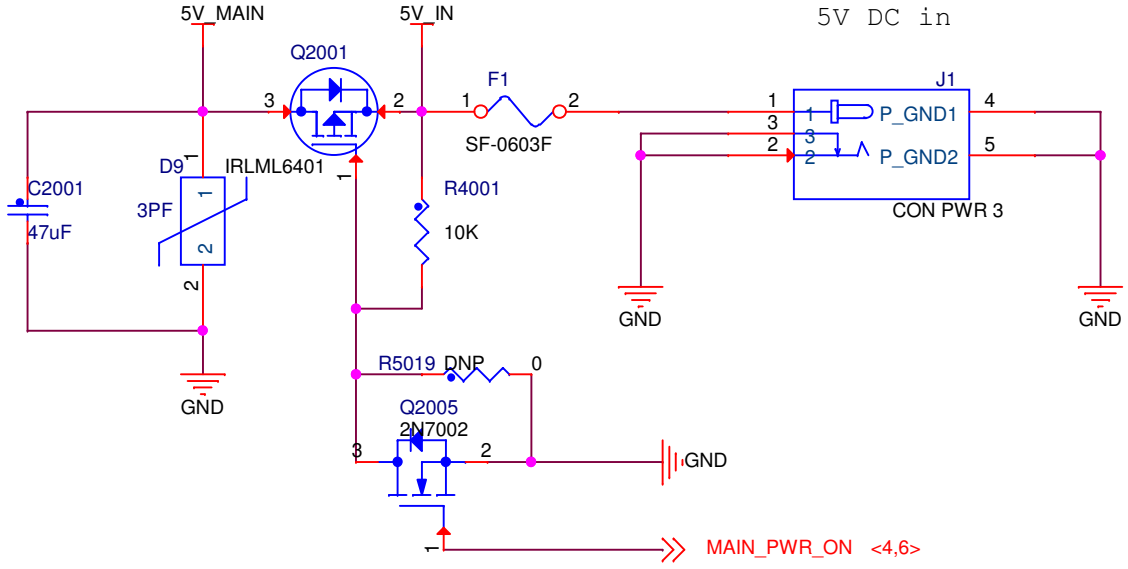

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Drawing Title:

i.MX51 Generic Reference Design

Page Title:

DC Input

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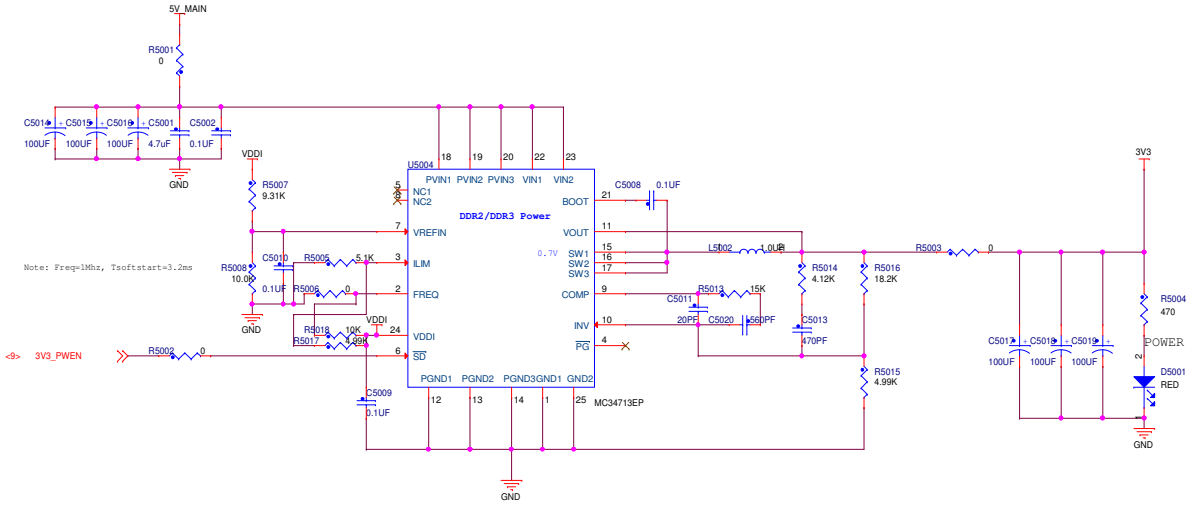
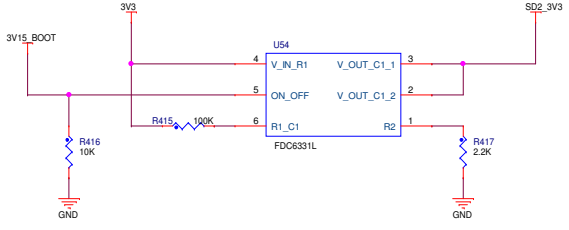
3V3 DC/DC Block



SD-2 High Side Power Switch



NOTE: This has been added to overcome the Atlas 3V15 supply current limitation for WiFi support on SDIO.

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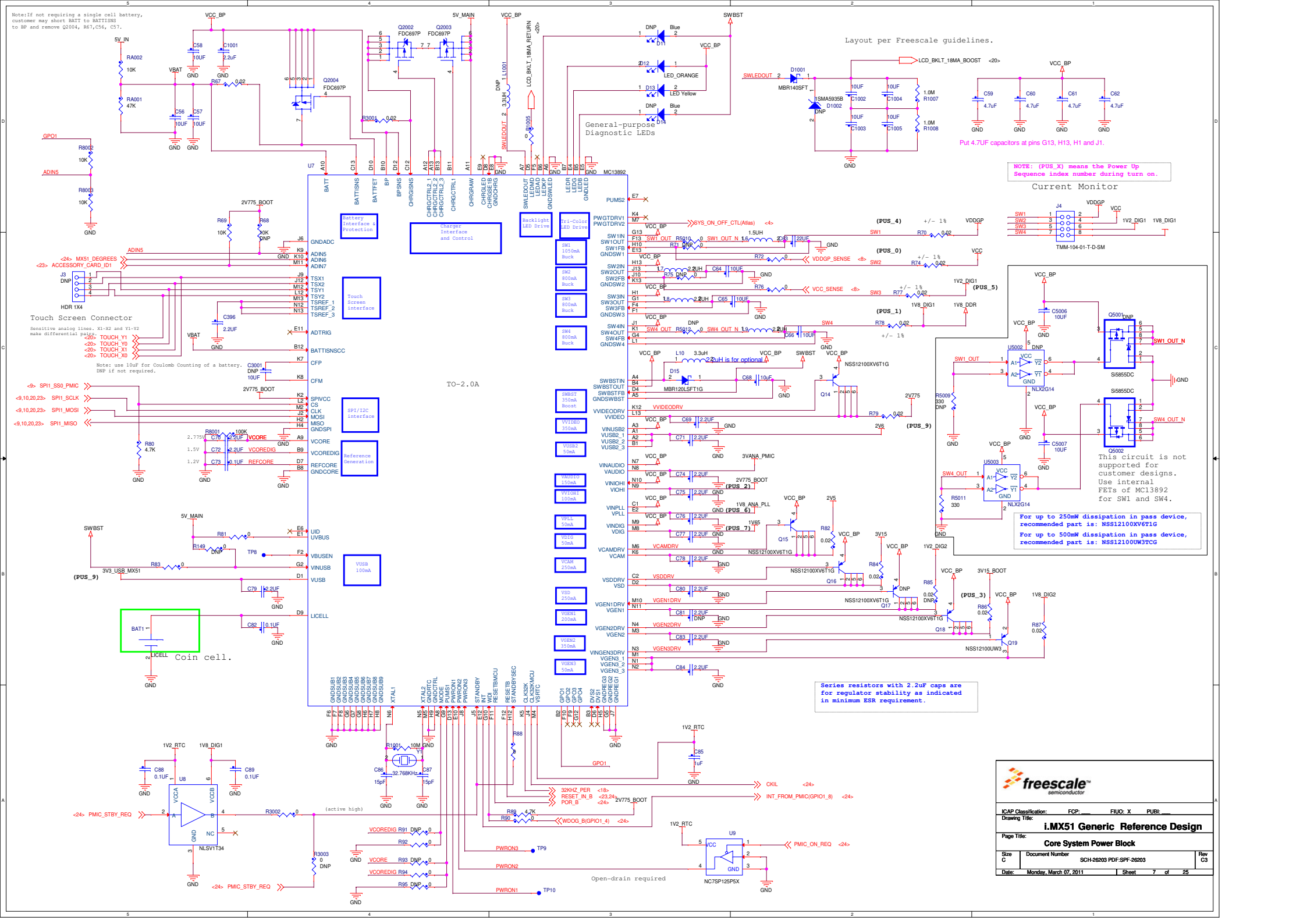
Note:If not requiring a single cell battery, customer may short BATT to BATTISNS to BP and remove Q2004, R67,C56, C57.
Layout per Freescale guidelines.
General-purpose Diagnostic LEDs
Put 4.7UF capacitors at pins G13, H13, H1 and J1.
NOTE: (PUS_X) means the Power Up Sequence index number during turn on.
Current Monitor
Touch Screen Connector
Coin cell.
TO-2.0A
Open-drain required
Series resistors with 2.2uF caps are for regulator stability as indicated in minimum ESR requirement.
This circuit is not supported for customer designs. Use internal FETs of MC13892 for SW1 and SW4.
For up to 250mW dissipation in pass device, recommended part is: NSS12100XV6T1G
For up to 500mW dissipation in pass device, recommended part is: NSS12100UW3TCG
Battery Interface & Protection
Charger Interface and Control
Backlight LED Drive
Tri-Color LED Drive
Touch Screen Interface
SPI/I2C Interface
Reference Generation
SW1 1050mA Buck
SW2 800mA Buck
SW3 800mA Buck
SW4 800mA Buck
SWBST 350mA Boost
VVIDEO 350mA
VUSB2 50mA
VAUDIO 150mA
VVIOHI 100mA
VPLL 50mA
VDIG 50mA
VCAM 250mA
VUSB 100mA
VSD 250mA
VGEN1 200mA
VGEN2 350mA
VGEN3 50mA
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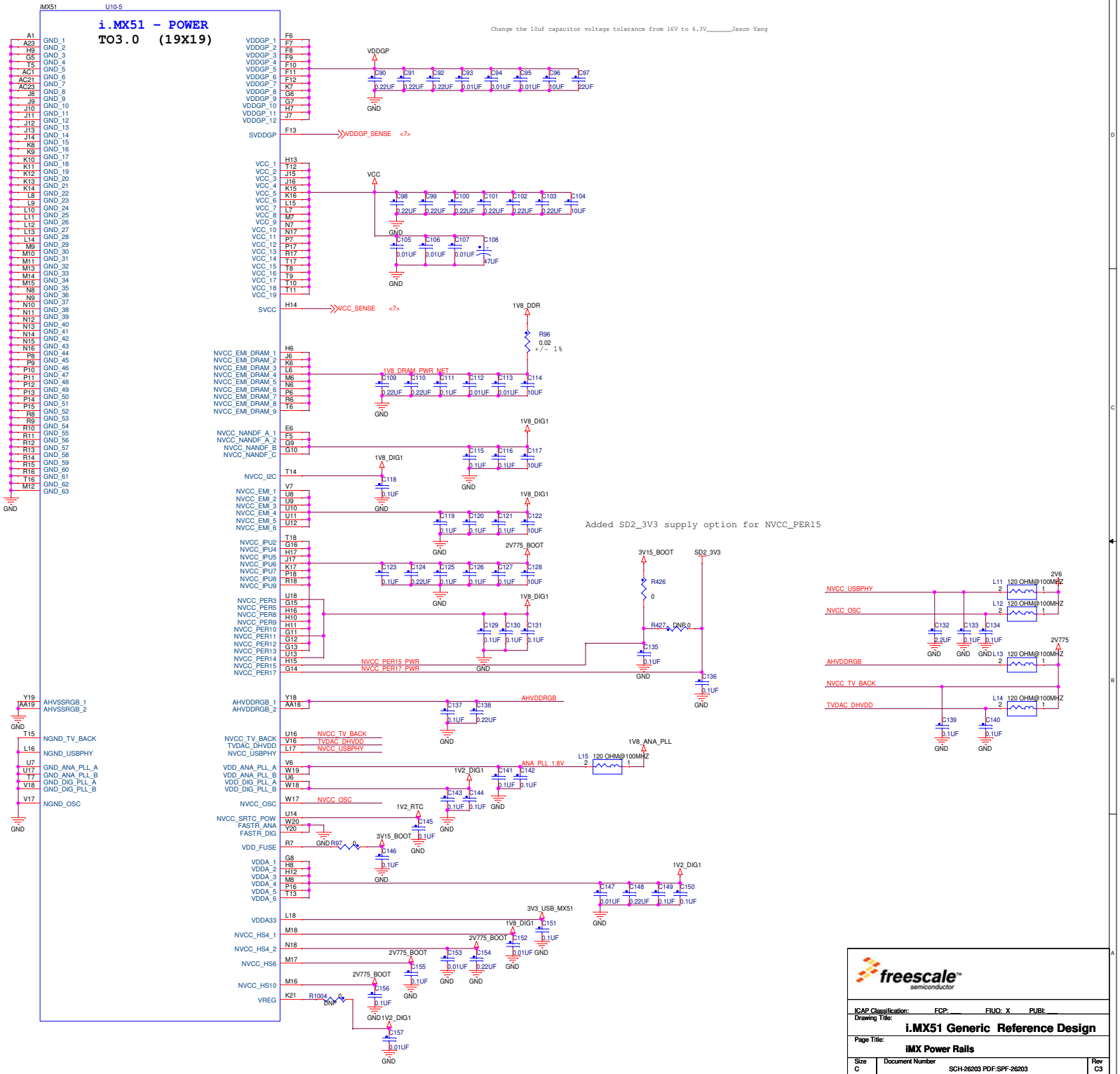
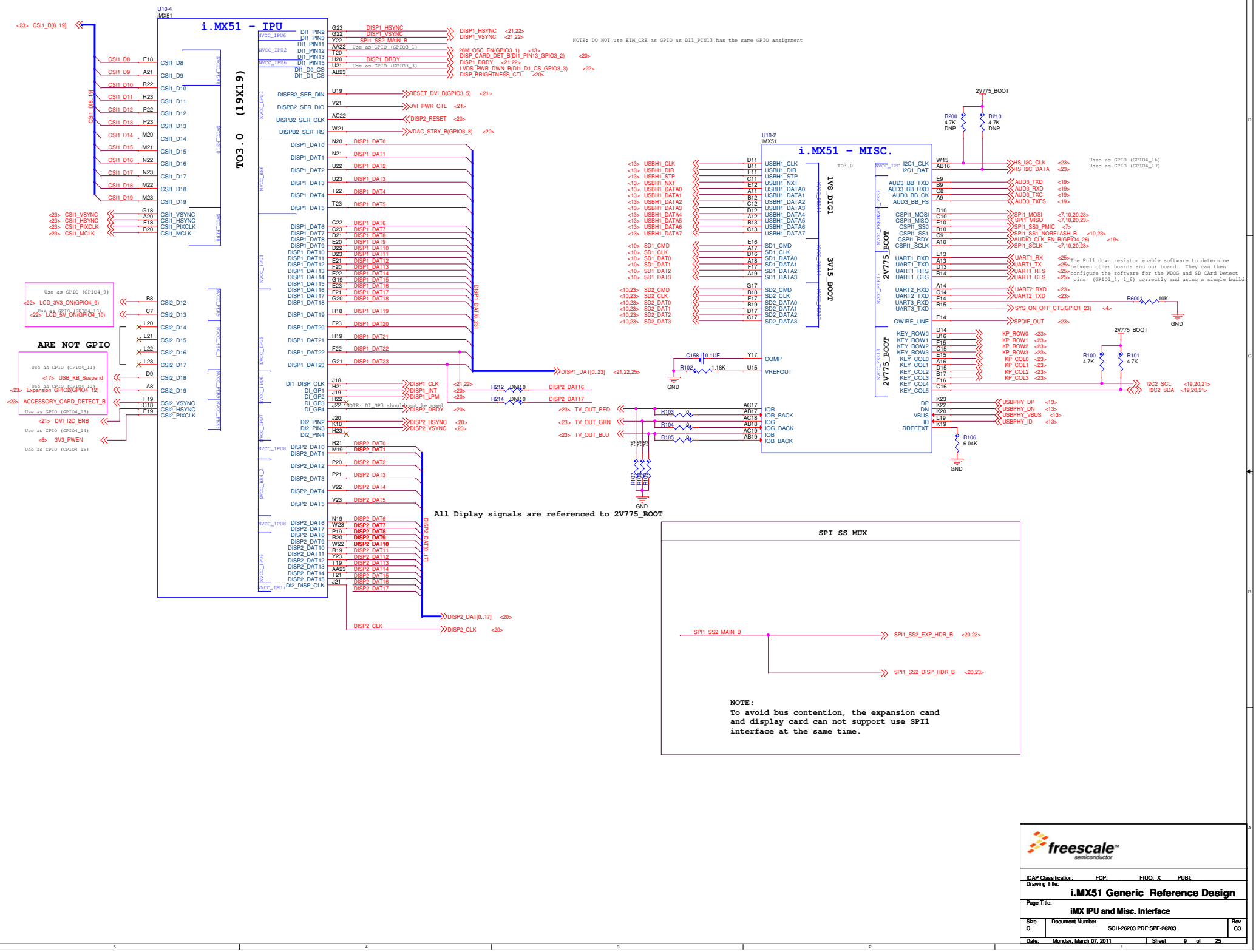
i.MX51 – POWER
TO3.0 (19X19)

Change the 10uf capacitor voltage tolerance from 16V to 6.3V_____Jason Yang

Added SD2_3V3 supply option for NVCC_PER15




i.MX51 - IPU
TO3.0 (19X19)
i.MX51 - MISC.
ARE NOT GPIO
All Diplay signals are referenced to 2V775_BOOT
SPI SS MUX
NOTE:
To avoid bus contention, the expansion cand
and display card can not support use SPI1
interface at the same time.
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FCP:
FIUO: X
PUBI:
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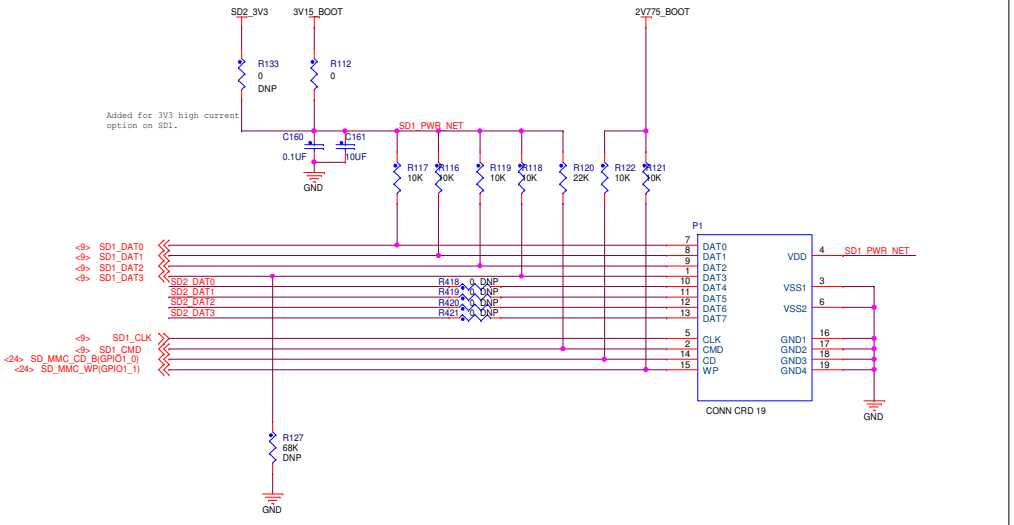
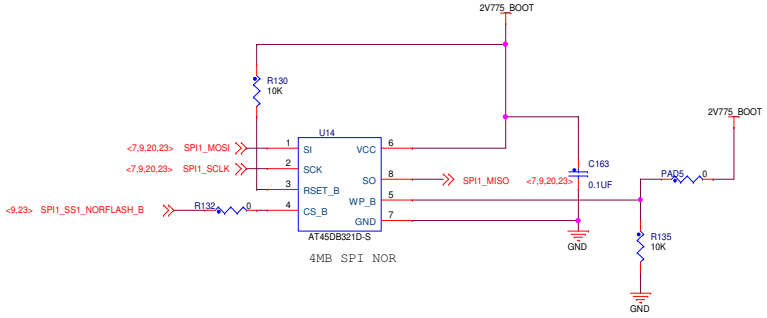
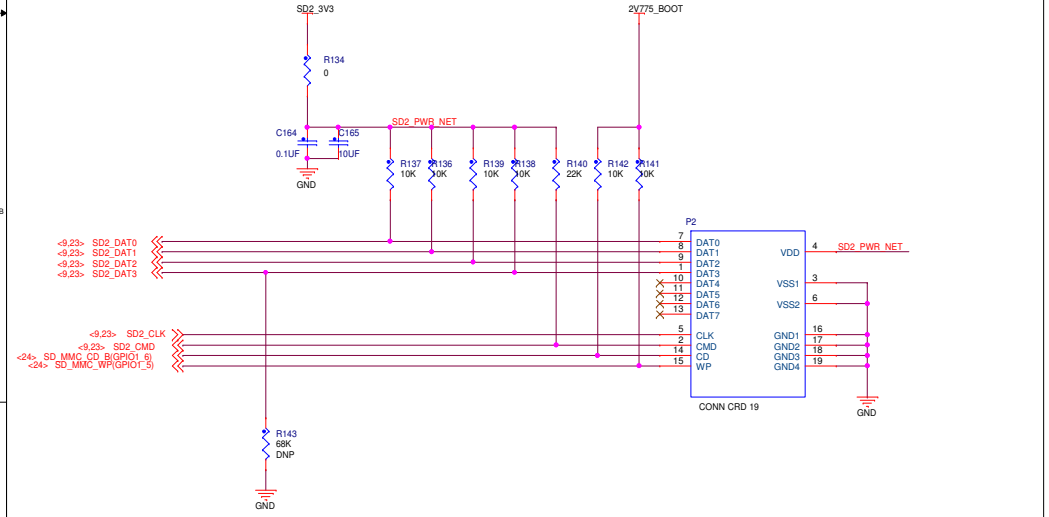
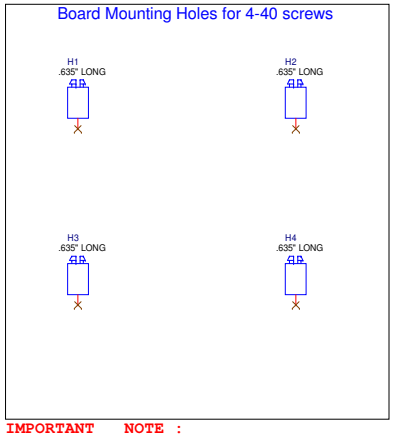
SD1/MMC1 : BOOT Port.





High Current SDIO Peripheral Port





IMPORTANT NOTE :

Use non-conducting nut/bolts to mount the board on a metallic chasis connected to external GND. Not doing so may cause board damage due to GND potential difference.

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We can use -8E or -6E

i.MX51 - MEMORY INTERFACE

U10-1
iMX51

EMI

DDR

NAND FLASH

Bank-1 Lower_Half

Bank-2 Lower_Half

Bank-1 Upper_Half

Bank-2 Upper_Half

DDR2 MEMORY

EDE1116AEBG

NOTE: DO NOT use EIM_CRE as GPIO as DI1_PIN13 has the same GPIO assignment

NOTE:
DDR data pins can be swapped for improved routing according to the following rules:

1) Data pins can be swapped within each byte
2) Data bytes can be swapped
3) DQMx and DQSx must follow each byte

When swapping bytes 0 or 1 into 2 or 3, must then use 32 bit access. Cannot use 16-bit access.

R148 should be on TOP side

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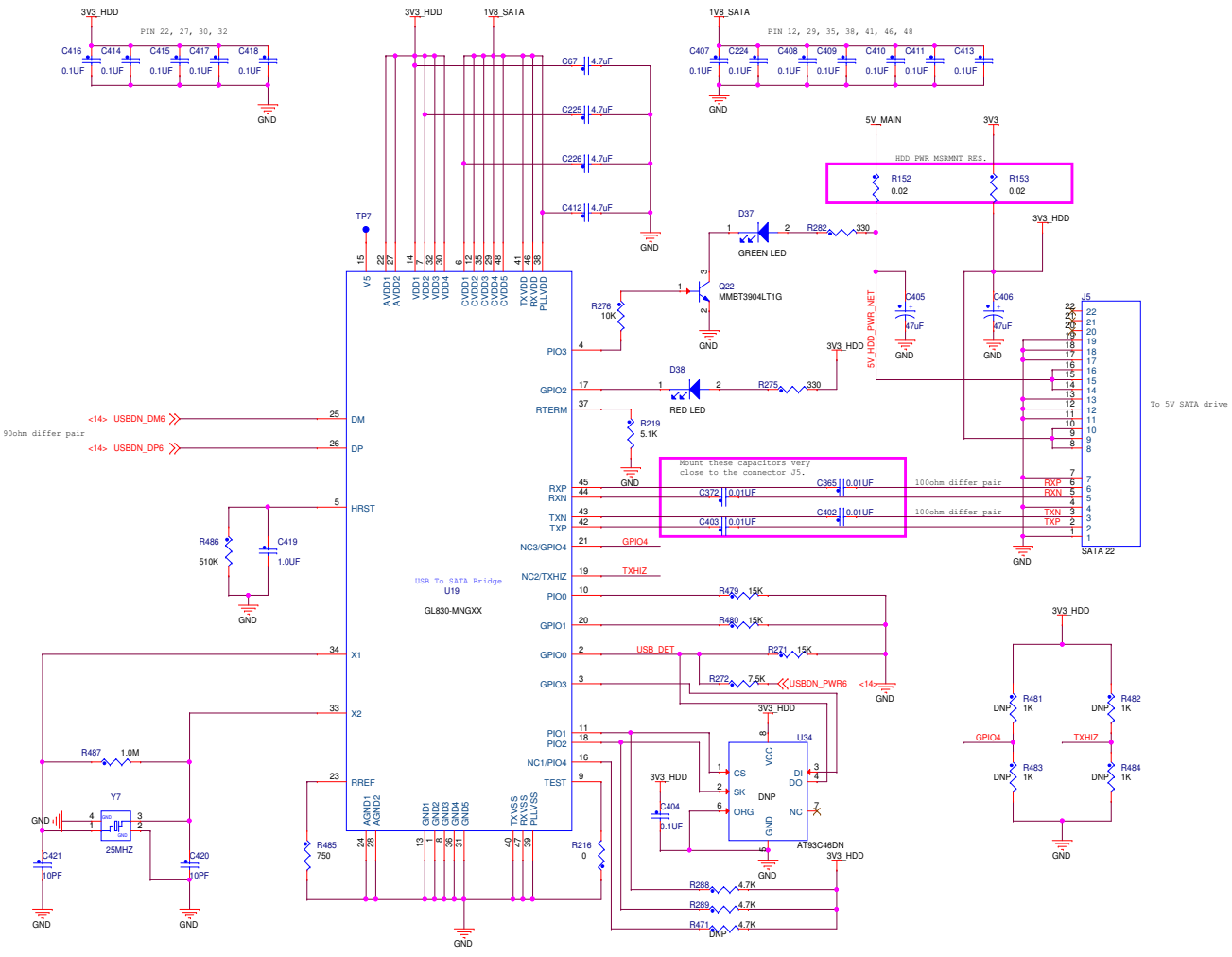
SATA HDD



NOTE:
There are 2 on-chip regulators in GL830. One is 5V-to-3.3V and the other is 3.3V-to-1.8V.
When supplied by 3.3V, the 5V supply pin should be left floating. The 1.8V is generated on-chip by the 3.3V supply.

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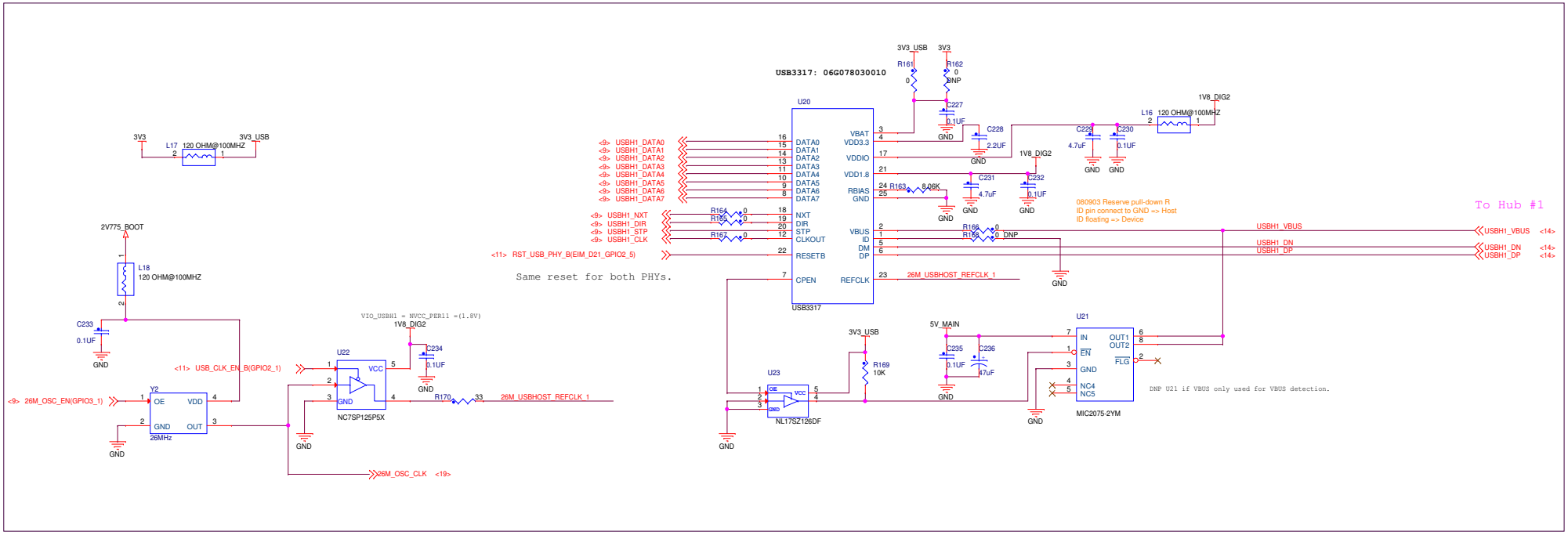
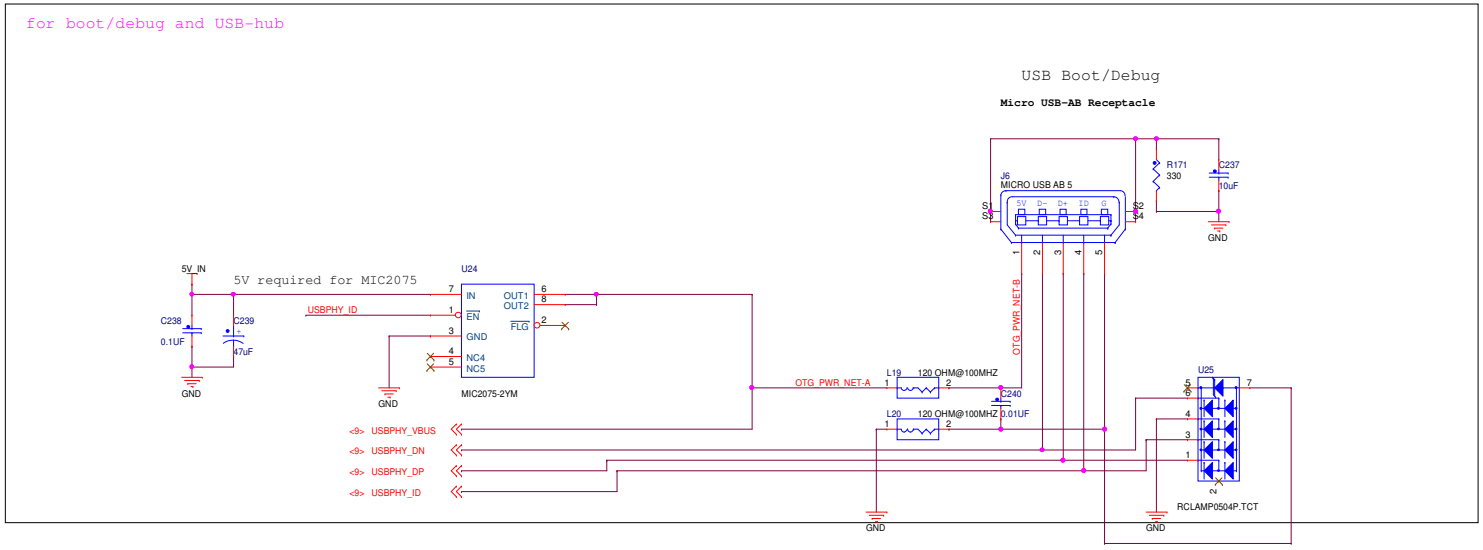
USB ULPI Host 1

to USB hub



USB on-chip OTG PHY

for boot/debug and USB-hub



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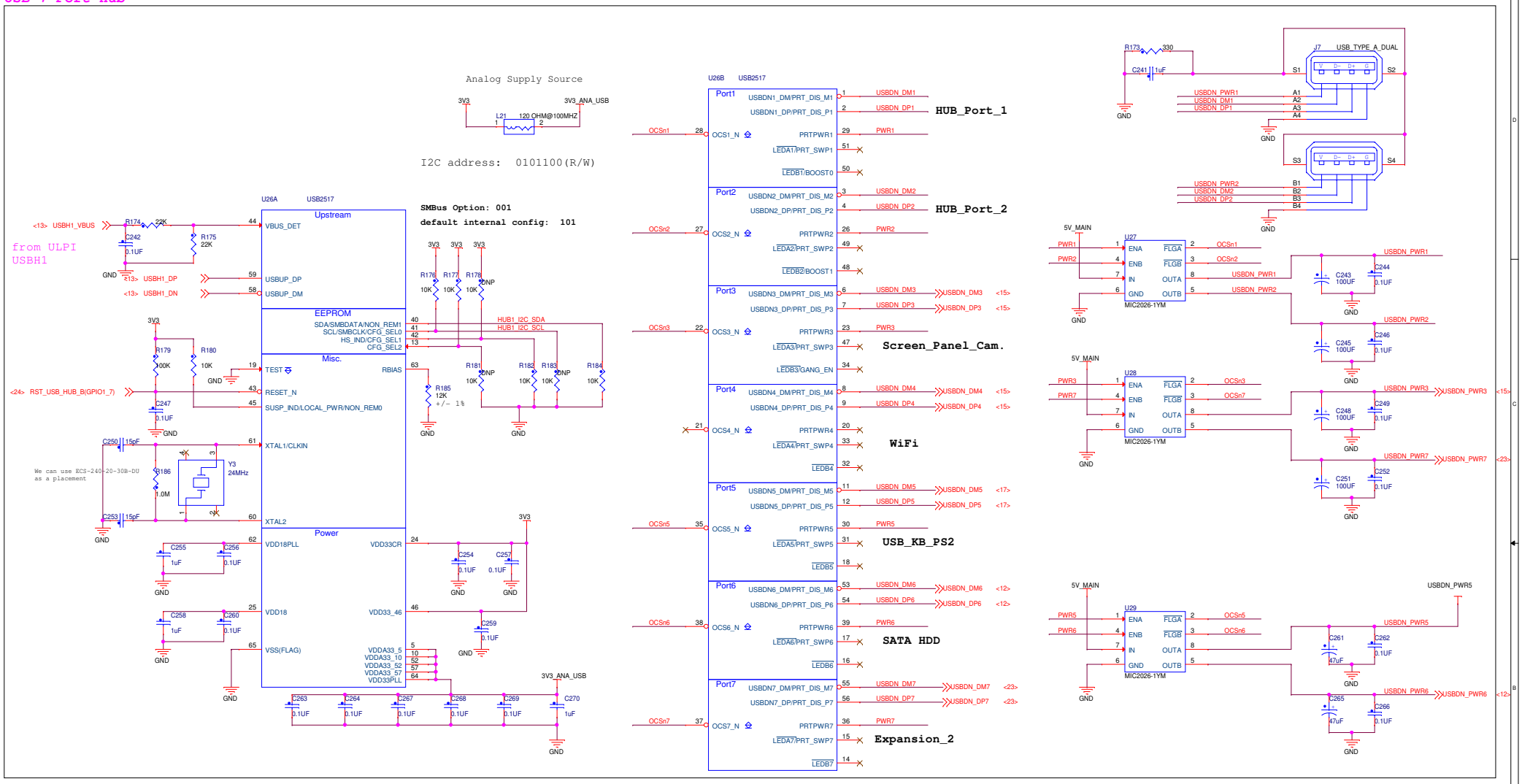
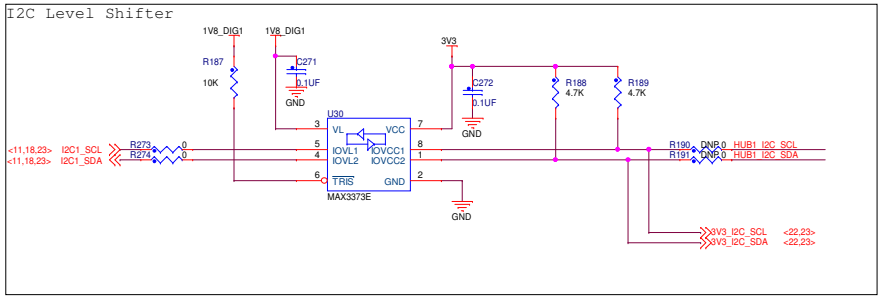
USB 7-Port Hub





USB1: Hub_Port_1
USB2: Hub_Port_2
USB3: LCD_Panel_Camera
USB4: WLAN
USB5: Key_Board and Touch Pad Controller
USB6: SATA HDD
USB7: USB on Expansion Header :: Intended for Video-In module/other type of peripheral

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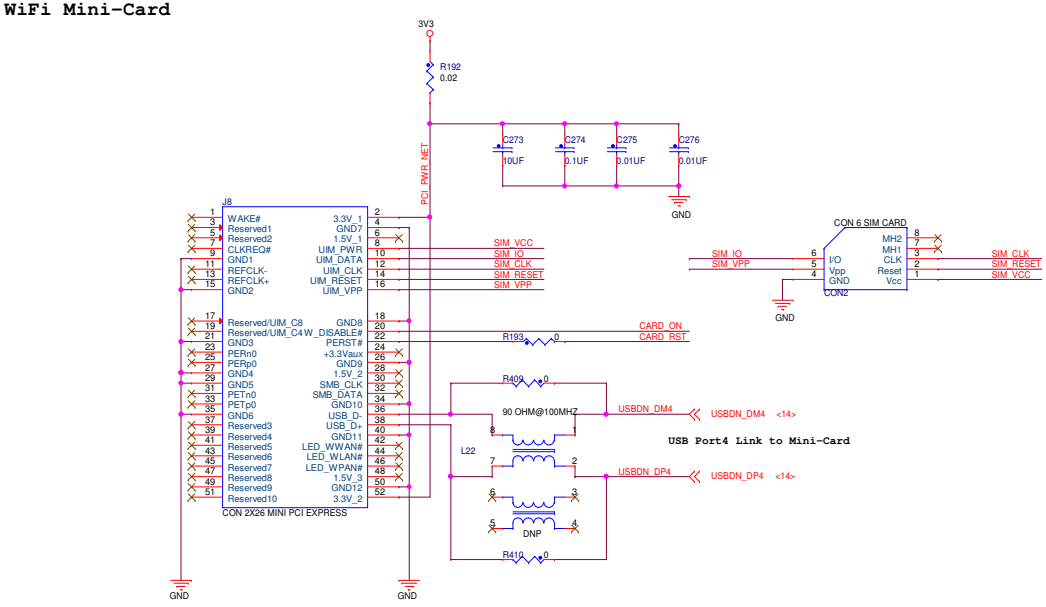
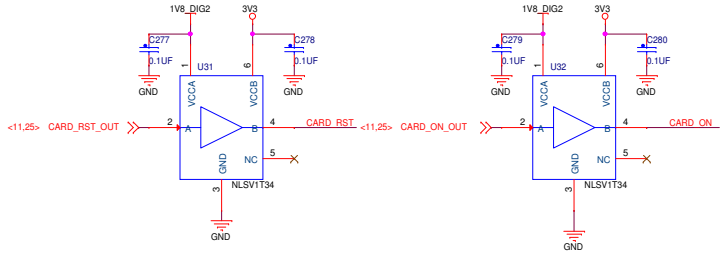
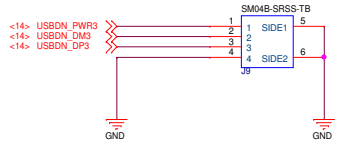
WiFi Mini-Card



This connector is for WIFI/Bluetooth module



On-Board USB Camera



freescale semiconductor		
ICAP Classification: FCP: ___ FIUO: X PUBI: ___		
Drawing Title: i.MX51 Generic Reference Design		
Page Title: USB Peripherals		
Size C	Document Number SCH-26203 PDF:SPF-26203	Rev C3
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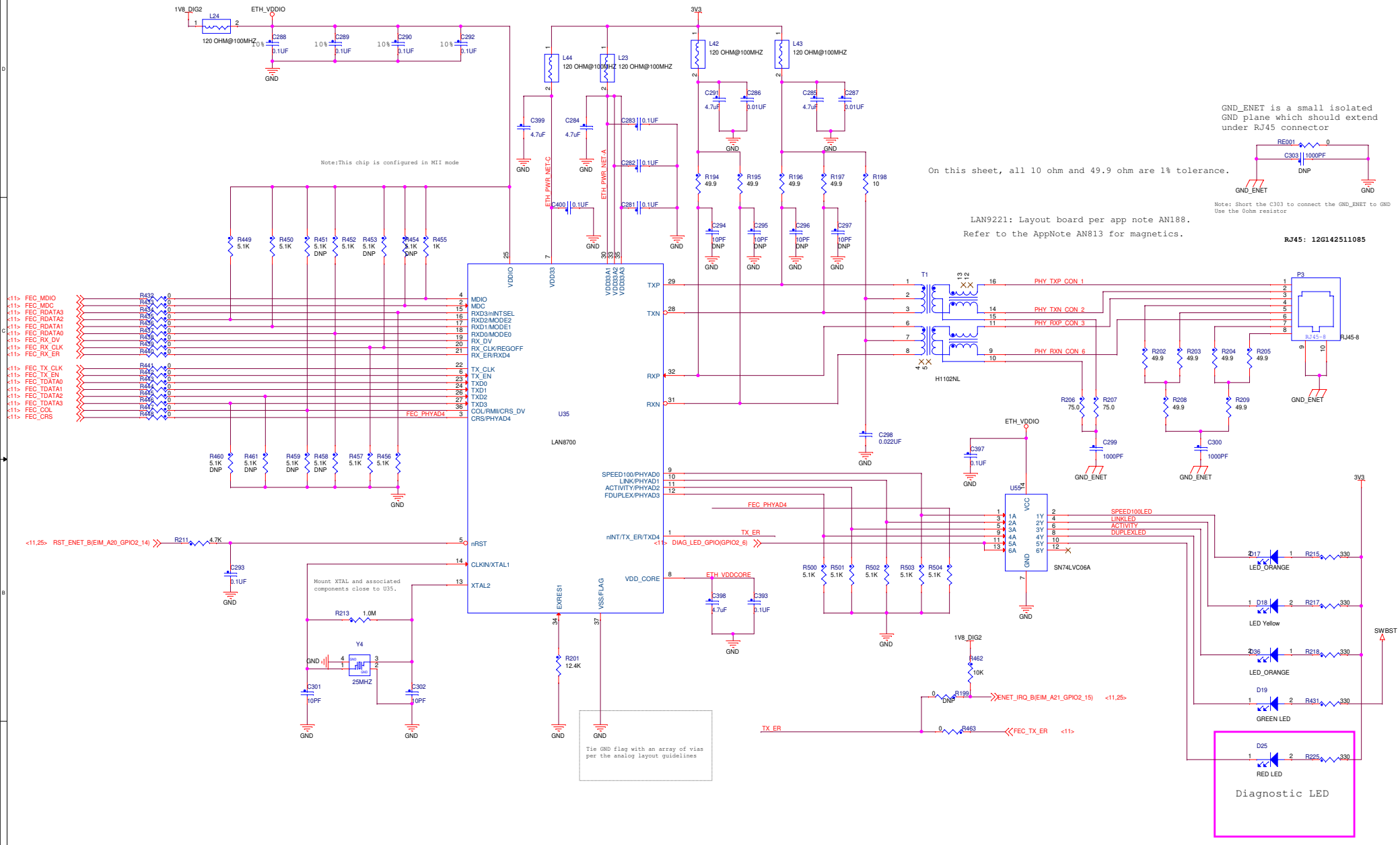
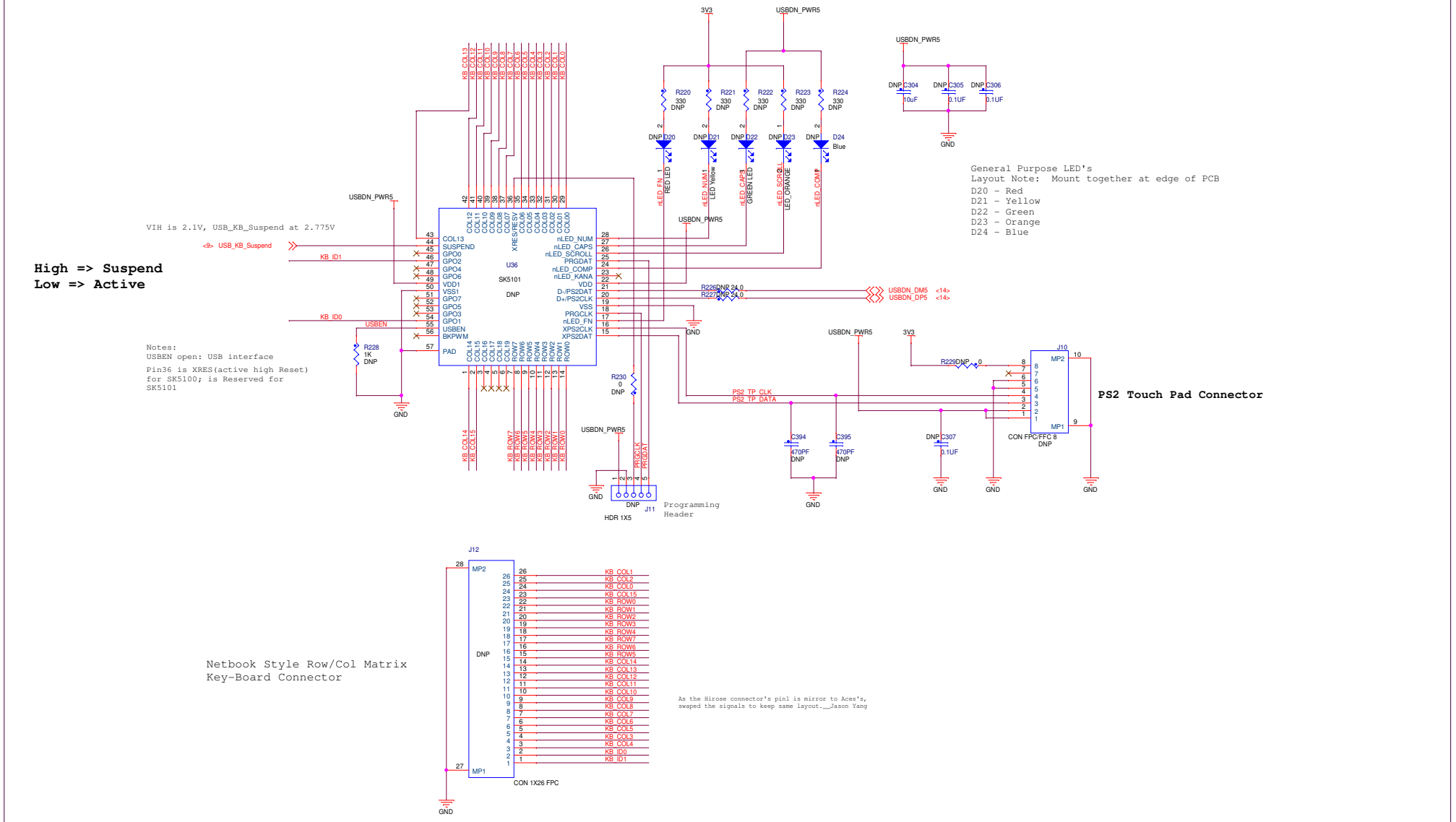
Ethernet Transceiver



ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	i.MX51 Generic Reference Design		
Page Title:	Ethernet PHY		
Size: C	Document Number: SCH-26203 PDF:SPF-26203		Rev: C3
Date: Monday, March 07, 2011		Sheet 16 of 25	

PS2 Touch Pad and KeyBoard Controller



ICAP Classification:	FCP: ___	FIUO: X	PUBI: ___
Drawing Title:	i.MX51 Generic Reference Design		
Page Title:	USB Keyboard and TouchPad		
Size: C	Document Number: SCH-26203 PDF:SPF-26203		Rev: C3
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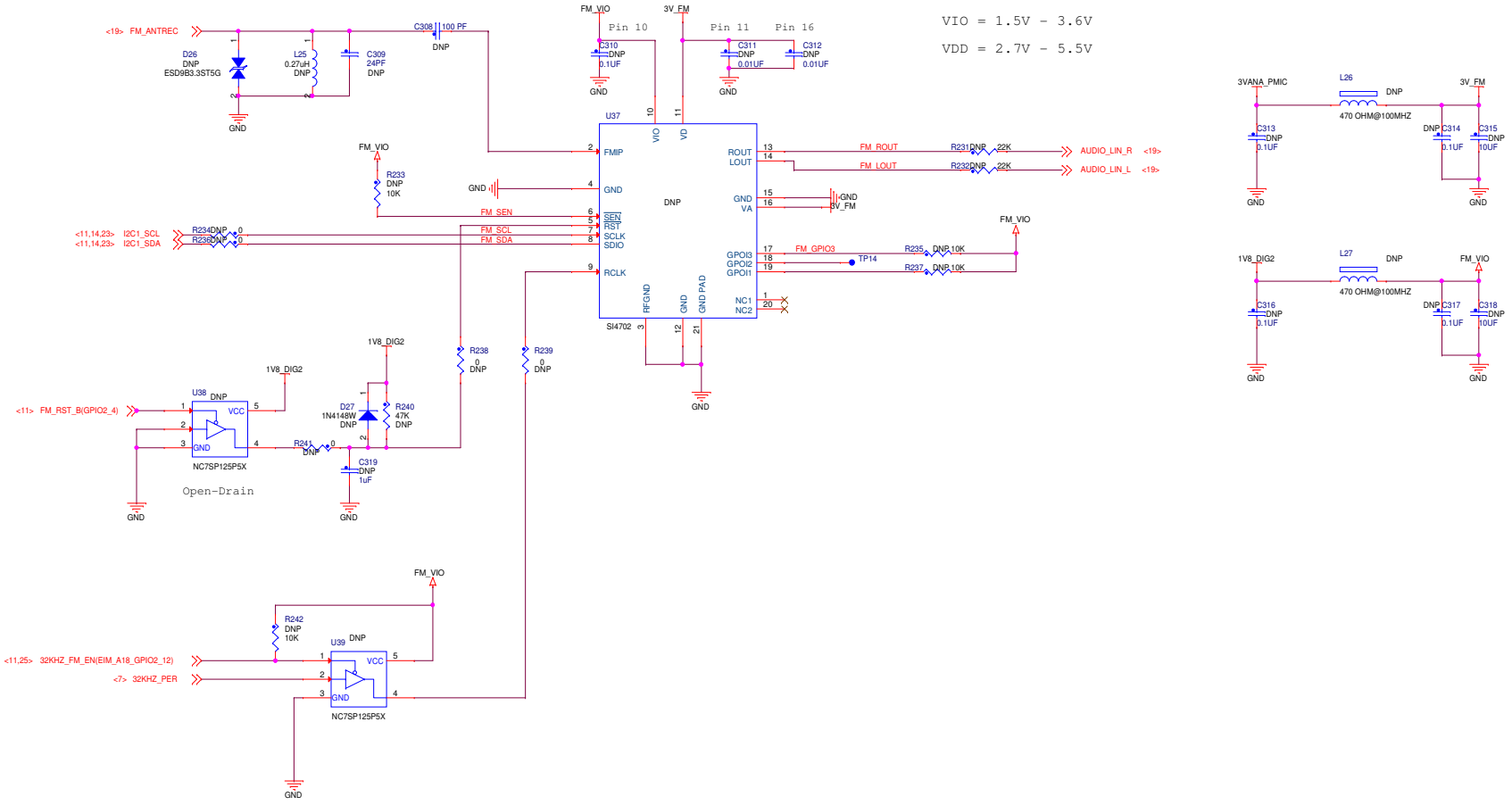
FM Receiver



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **i.MX51 Generic Reference Design**

Page Title: **FM Radio Receiver**

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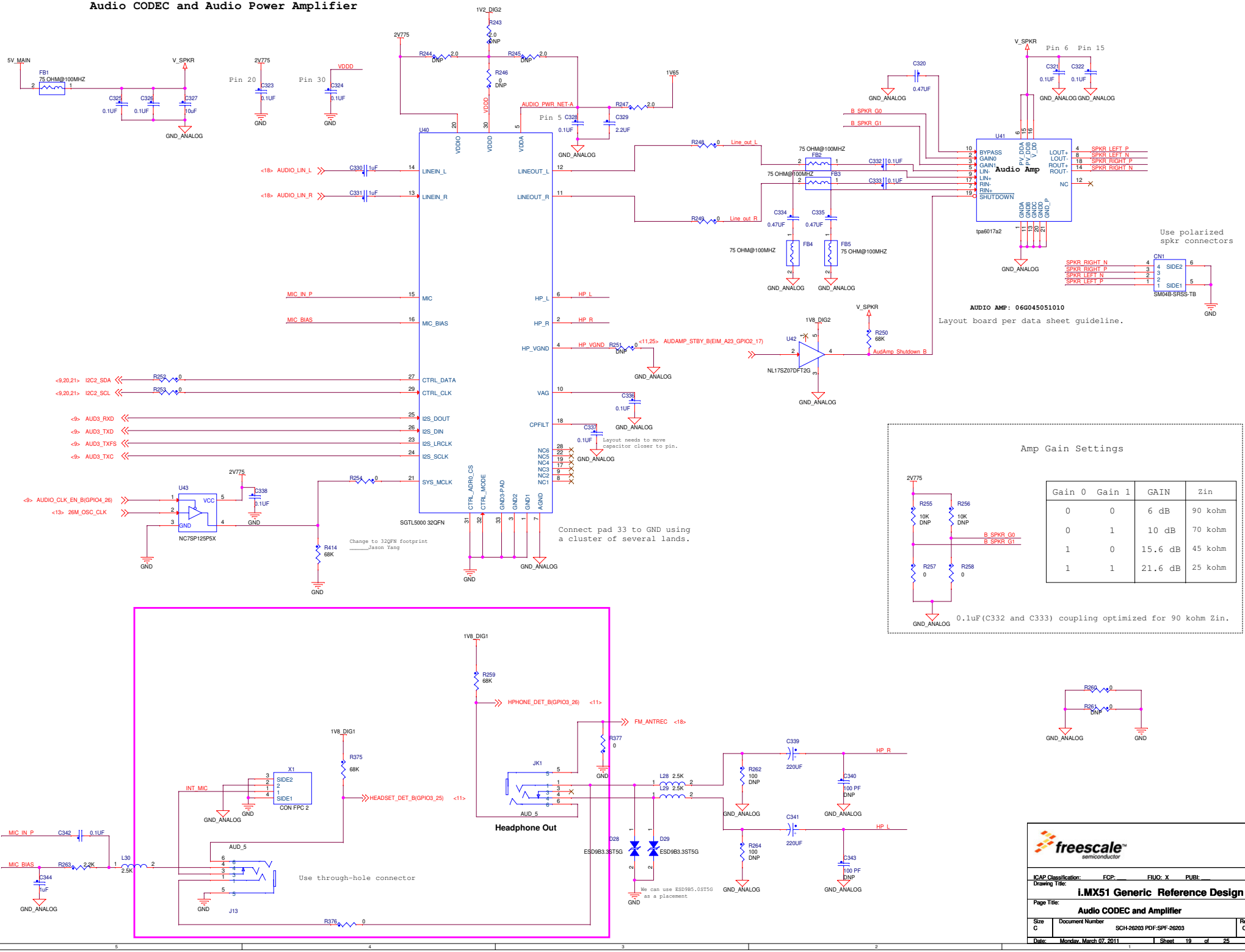
Audio CODEC and Audio Power Amplifier



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ICAP Classification:	FCP:	FIUO: X	PUBI:
Drawing Title:	i.MX51 Generic Reference Design		
Page Title:	Audio CODEC and Amplifier		
Size: C	Document Number: SCH-26203 PDF:SPF-26203		Rev: C3
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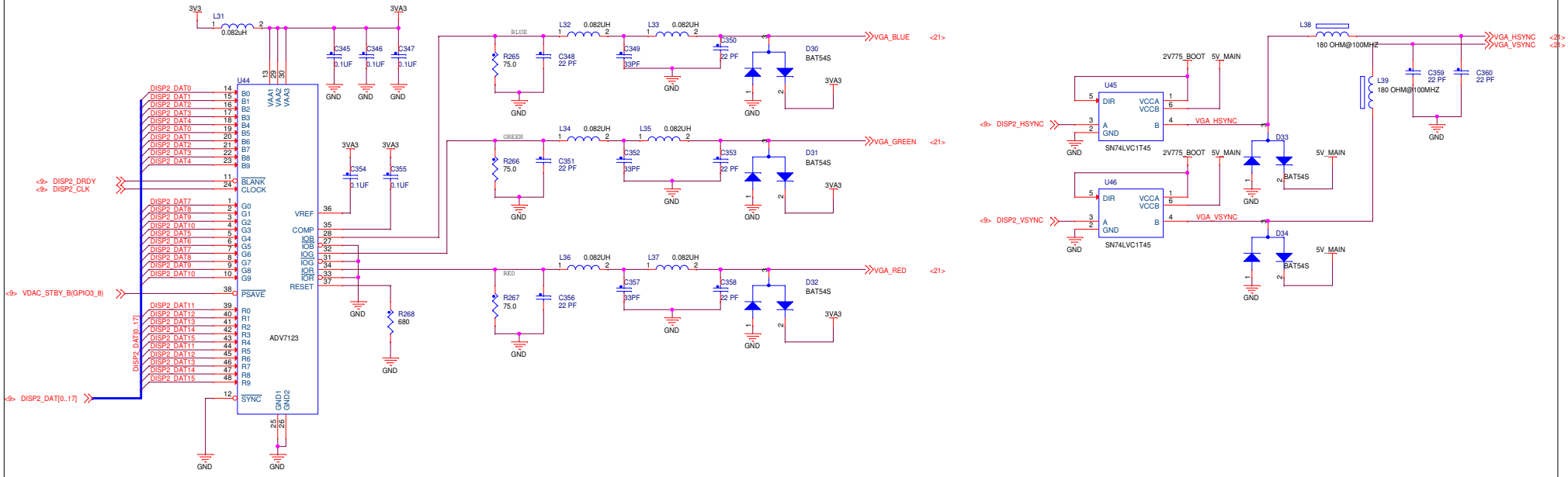
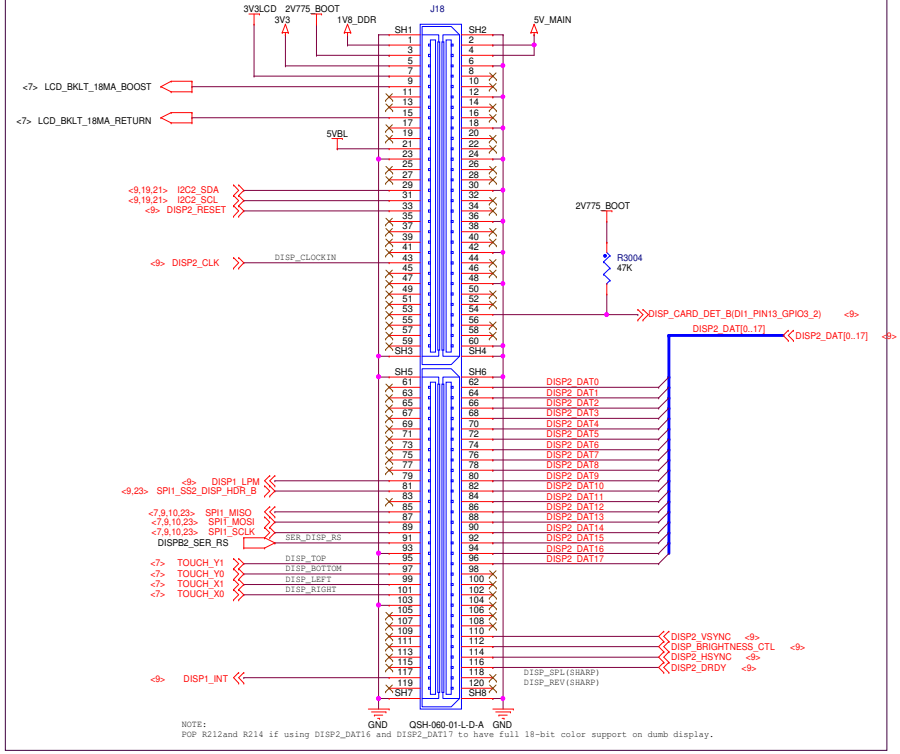
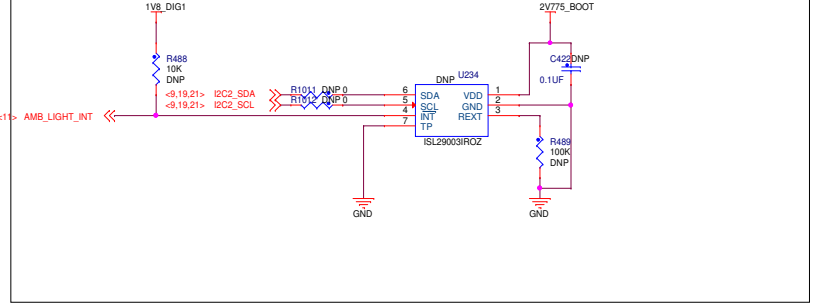
VIDEO DAC



16/18-bit Parallel Dumb Display Expansion Port on Display-Port-2



Ambient Light Sensor



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ICAP Classification:	FCP: ___ FIUO: X PUBI: ___
Drawing Title:	i.MX51 Generic Reference Design
Page Title:	display connector + Light sensor
Size: C	Document Number: SCH-26203 PDF:SPF-26203 Rev: C3
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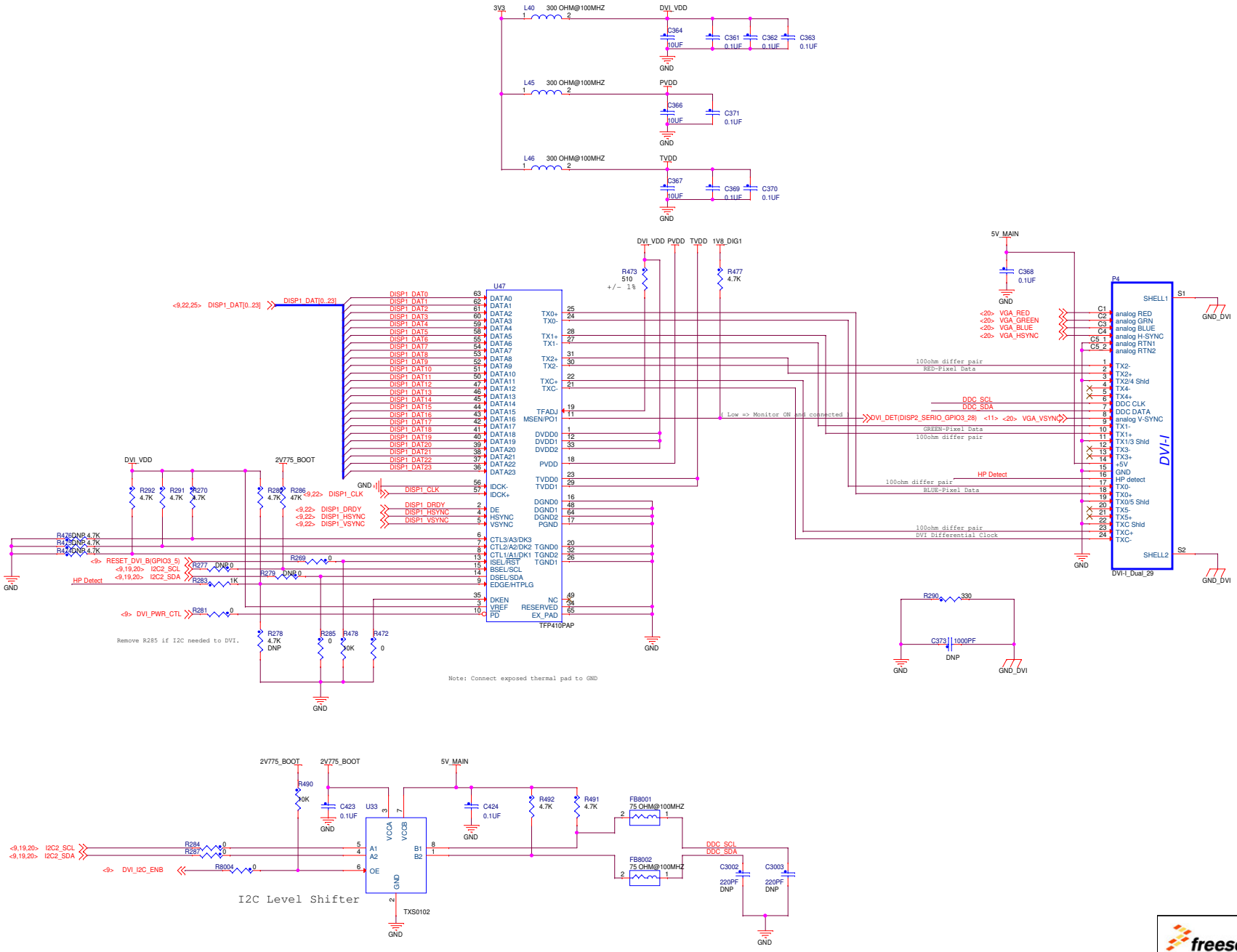
DVI Transmitter



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **i.MX51 Generic Reference Design**

Page Title: **DVI-I Display**

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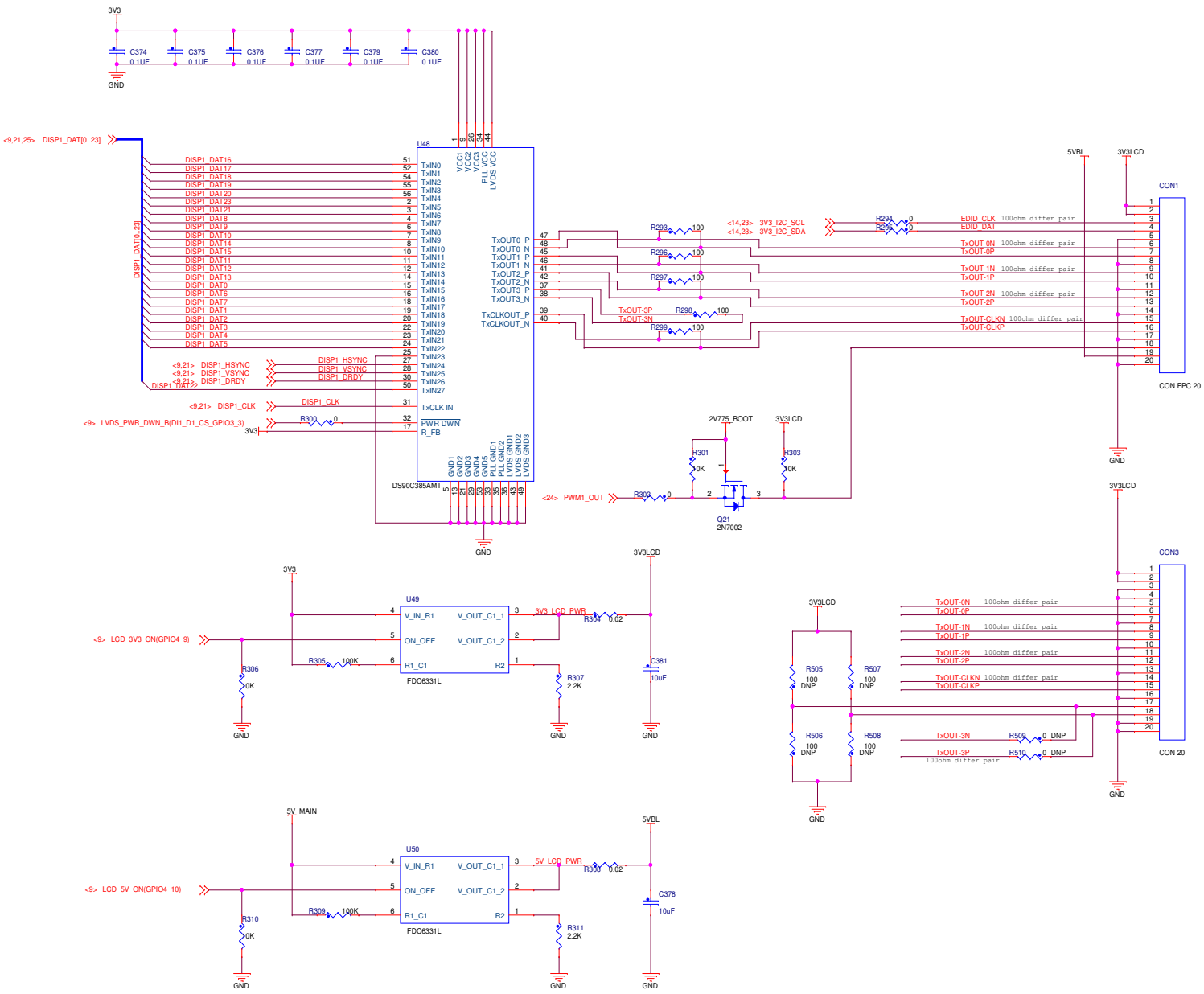
LVDS Display



ICAP Classification:	FCP: ___ FIUO: X PUBI: ___	
Drawing Title:	i.MX51 Generic Reference Design	
Page Title:	LVDS Display	
Size: C	Document Number: SCH-26203 PDF:SPF-26203	Rev: C3
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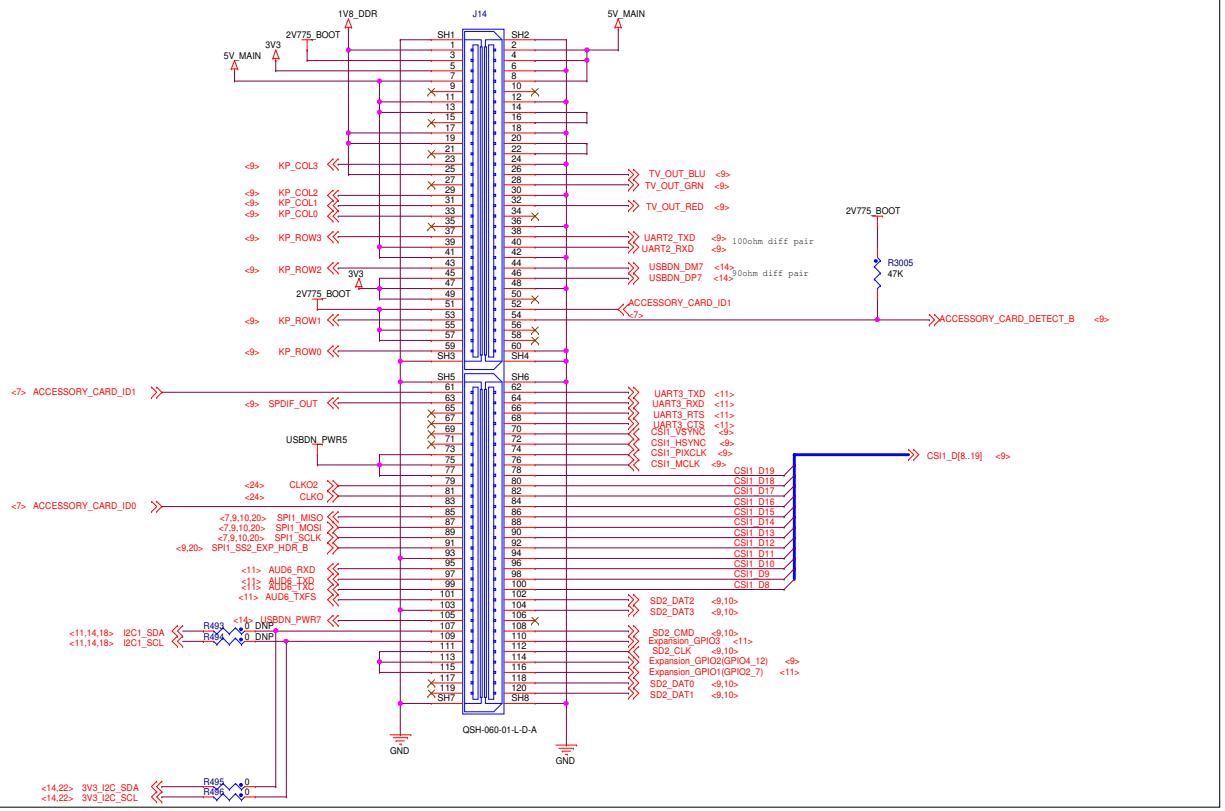
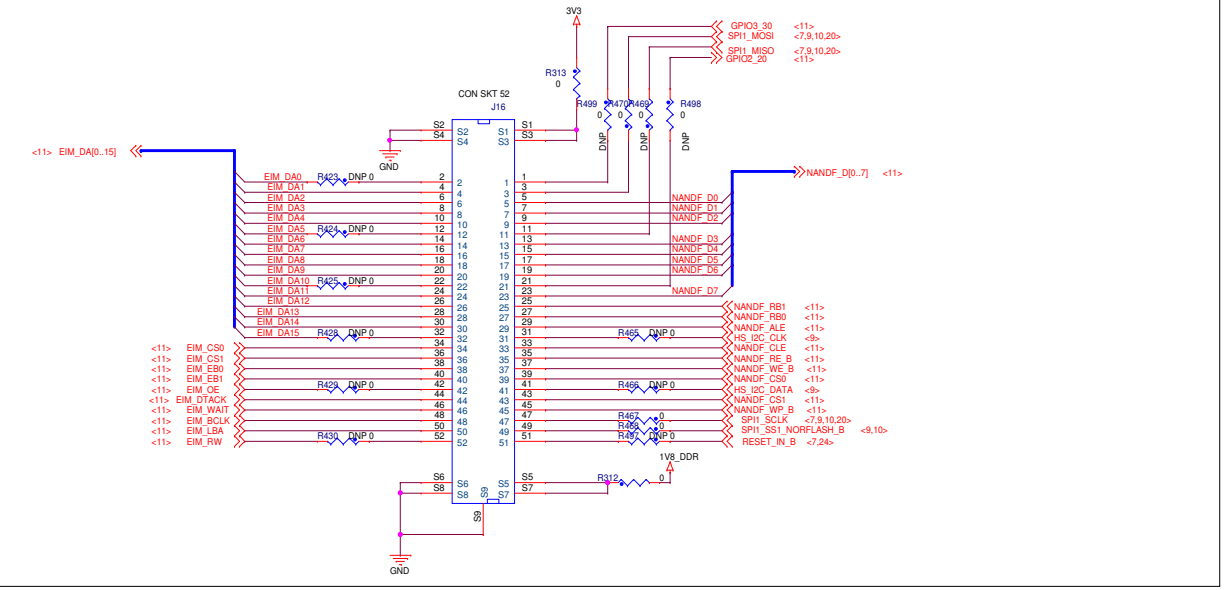
Peripheral Expansion Board Header



EMI and NAND x8 Expansion Port



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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **i.MX51 Generic Reference Design**

Page Title: **Expansion Header**

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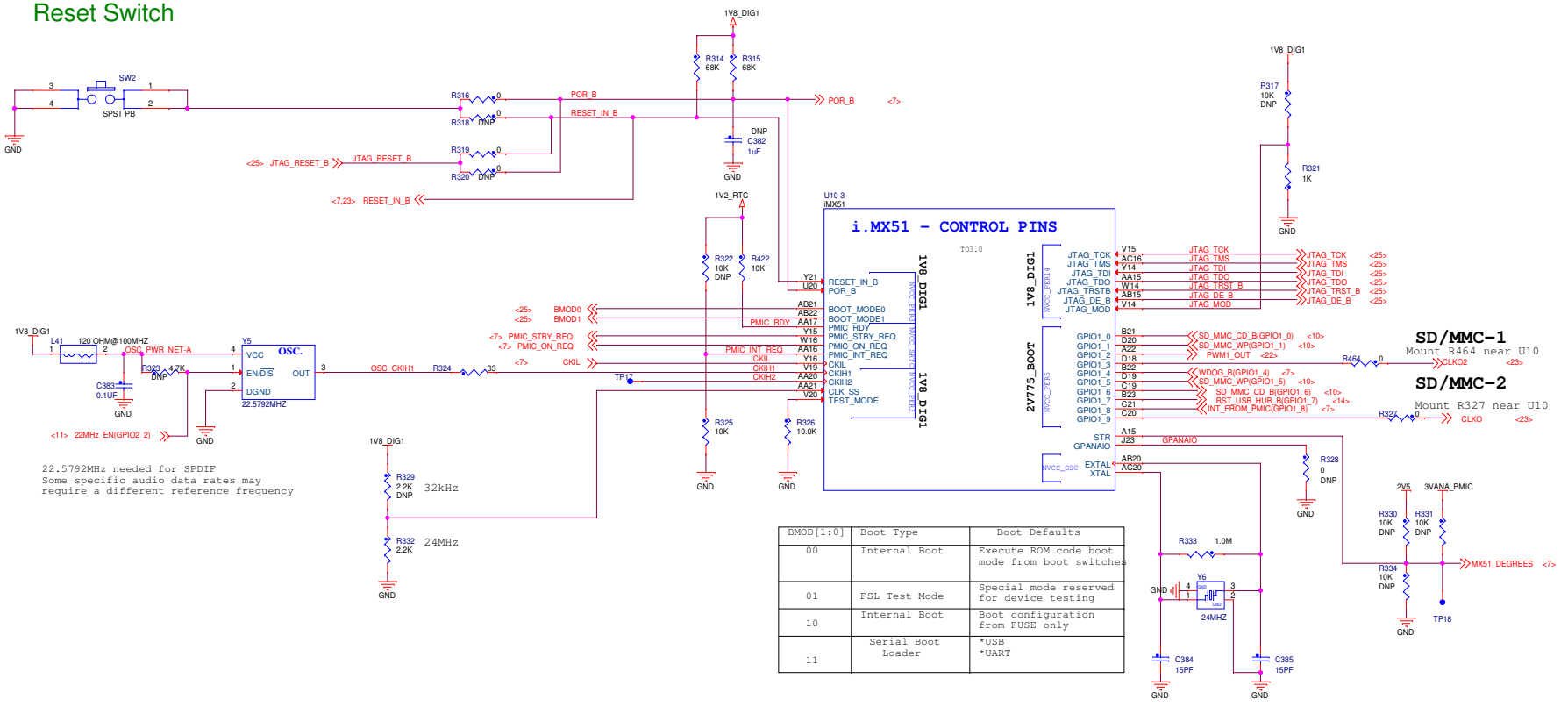
i.MX Control

Reset Switch



BMOD[1:0]	Boot Type	Boot Defaults
00	Internal Boot	Execute ROM code boot mode from boot switches
01	FSL Test Mode	Special mode reserved for device testing
10	Internal Boot	Boot configuration from FUSE only
11	Serial Boot Loader	*USB *UART

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **i.MX51 Generic Reference Design**

Page Title: **iMX Control**

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BOOT Mode Selection

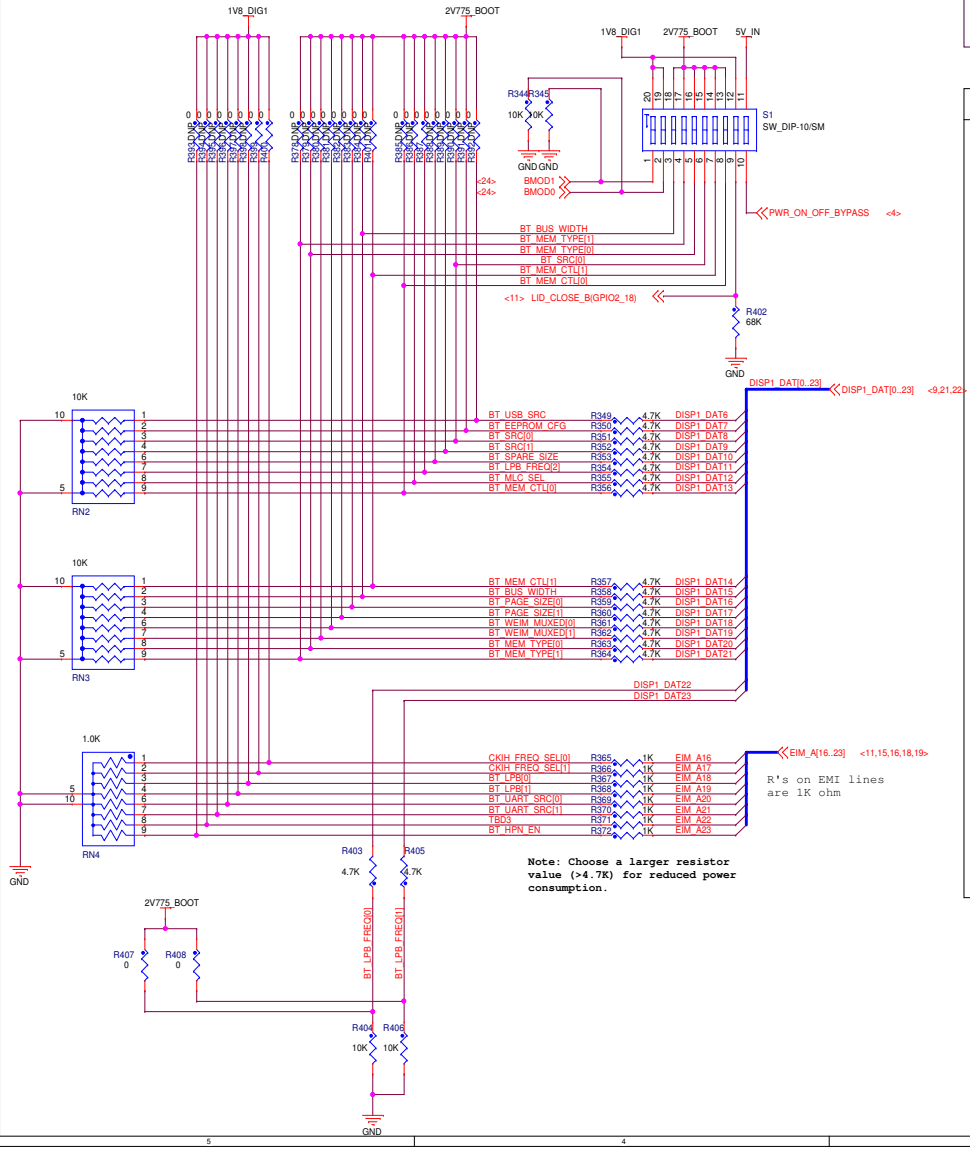
Switch S1 Functions

	Position 1	Position 2	Position 3	Position 4	Position 5	Position 6	Position 7	Position 8	Position 9	Position 10
	BOOT_MODE[1:0]		BT_BUS_WIDTH	BT_MEM_TYPE[1:0]		BT_SRC[0]	BT_MEM_CTL[1:0]		LID_CLOSE_B	PWR_BYP
SPI-NOR	0	0	1	1	1	0	1	1	X	X
MMC-1	0	0	0	0	0	0	1	1	X	X
MMC-2	0	0	0	0	0	1	1	1	X	X
UART-1	1	1	0	0	0	0	1	1	X	X
USB-OTG	1	1	0	0	0	0	1	1	X	X

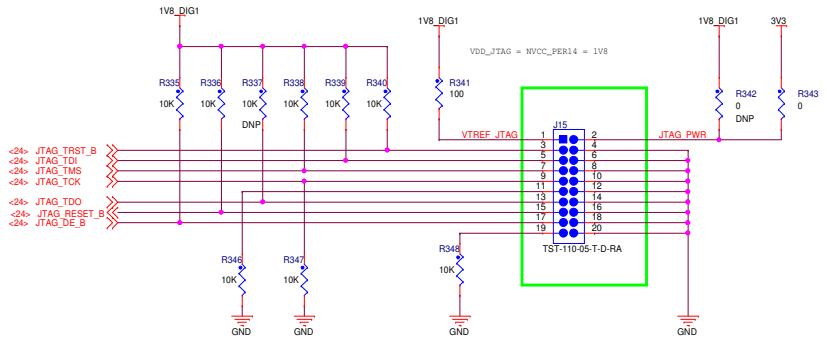
DIP Switch is 10-position. 0= off, 1 = on. See schematic sheet 26 for additional functions allowed by 0-ohm resistors.

Position 9 is for simulation of netbook lid open and close.

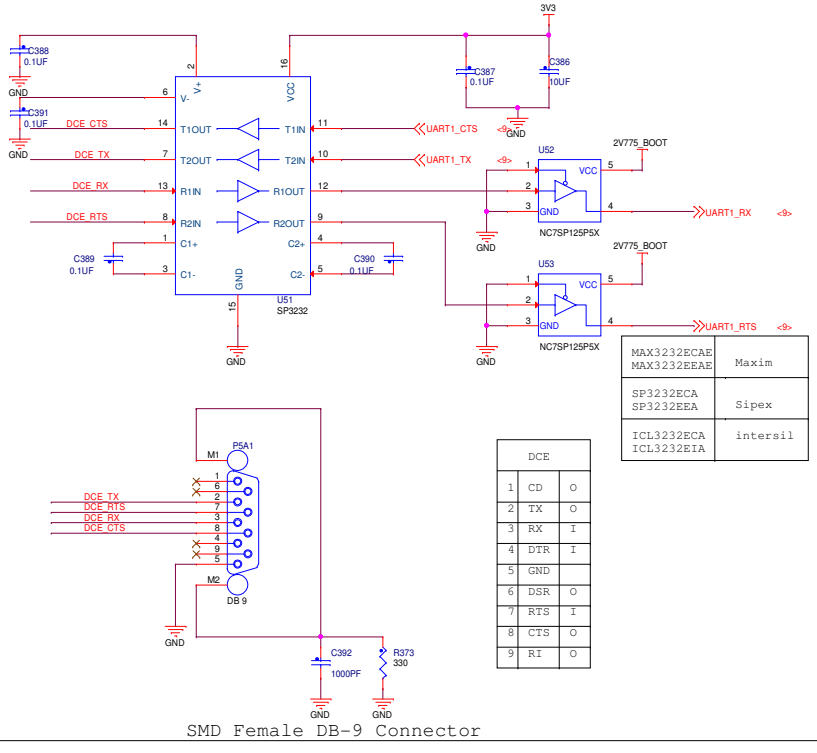
Position 10, when switched on, forces the system to power up as soon as power is applied. For normal operation, switch to off.



JTAG



Debug/BOOT UART



MAX3232ECAE MAX3232EEAE	Maxim
SP3232ECA SP3232EEA	Sipex
ICL3232ECA ICL3232EIA	intersil

DCE		
1	CD	O
2	TX	O
3	RX	I
4	DTR	I
5	GND	
6	DSR	O
7	RTS	I
8	CTS	O
9	RI	O

SMD Female DB-9 Connector

BMOD[1:0]	Boot Type	Boot Defaults
00	Internal Boot	Execute ROM code boot mode from boot switches
01	FSL Test Mode	Special mode reserved for device testing
10	Internal Boot	Boot configuration from FUSE only
11	Serial Boot Loader	*USB *UART

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ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **i.MX51 Generic Reference Design**

Page Title: **JTAG, DBG_UART, BOOT_Config**

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